

Form PTO-1390		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER P19797
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 09/600890		
INTERNATIONAL APPLICATION NO. PCT/JP99/00504	INTERNATIONAL FILING DATE 5 February 1999		PRIORITY DATE CLAIMED 26 February 1998	
TITLE OF INVENTION MULTILAYER PRINTED WIRING BOARD WITH FILLED VIAHOLE STRUCTURE TECHNICAL FIELD				
APPLICANT(S) FOR DO/EO/US Seiji SHIRAI, Kenichi SHIMADA, and Motoo ASAII				
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.				
<p>1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.</p> <p>2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.</p> <p>3. <input checked="" type="checkbox"/> This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).</p> <p>4. <input checked="" type="checkbox"/> A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.</p> <p>5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(C)(2))</p> <p>a. <input checked="" type="checkbox"/> is transmitted herewith (required only if not transmitted by the International Bureau).</p> <p>b. <input type="checkbox"/> has been transmitted by the International Bureau.</p> <p>c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US).</p> <p>6. <input checked="" type="checkbox"/> A Translation of the International Application into English (35 U.S.C. 371 (c)(2)).</p> <p>7. <input type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))</p> <p>a. <input type="checkbox"/> are transmitted herewith (required only if not transmitted by the International Bureau).</p> <p>b. <input type="checkbox"/> have been transmitted by the International Bureau.</p> <p>c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired.</p> <p>d. <input type="checkbox"/> have not been made and will not be made.</p> <p>8. <input type="checkbox"/> A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3))</p> <p>9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).</p> <p>10. <input checked="" type="checkbox"/> "Executed"</p> <p>11. <input type="checkbox"/> A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (U.S.C. 371(c)(5)).</p>				
Items 11. to 16. below concern other document(s) or information included:				
<p>11. <input type="checkbox"/> An information Disclosure Statement under 37 CFR 1.97 and 1.98.</p> <p>12. <input checked="" type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.</p> <p>13. <input checked="" type="checkbox"/> A FIRST preliminary amendment.</p> <p><input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment.</p> <p>14. <input type="checkbox"/> A substitute specification.</p> <p>15. <input type="checkbox"/> A change of power of attorney and/or address letter.</p> <p>16. <input checked="" type="checkbox"/> Other items or information: Cover Sheet and Copy of International Application as published in Japanese. PCT/RO/101-PCT Request(in Japanese). PCT Amendment (with one replacement page). PCT/IPA/409-International Preliminary Examination Report(in Japanese). PCT/IB/301. PCT/IB/304. PCT/IB/308. PCT/IB/332. PCT/ISA/210-International Search Report(in English and Japanese). Claim of Priority.</p>				

U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 09/600890		INTERNATIONAL APPLICATION NO. PCT/JP99/00504	ATTORNEY'S DOCKET NUMBER P19797
17. <input checked="" type="checkbox"/> The following fees are submitted:		CALCULATIONS PTO USE ONLY	
<p>Basic National Fee (37 CFR 1.492(a)(1)-(5)):</p> <p>Search report has been prepared by the EPO or JPO. \$ 840.00</p> <p>International preliminary examination fee paid to USPTO (37 CFR 1.482). \$ 670.00</p> <p>No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)). \$ 760.00</p> <p>Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO. \$ 970.00</p> <p>International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4). \$ 96.00</p>			
ENTER APPROPRIATE BASIC FEE AMOUNT = \$840.00			
<p>Surcharge of \$130.00 for furnishing the oath or declaration later than <u>20</u> <u>30</u> months from the earliest claimed priority date (37 CFR 1.492(e)).</p>			
Claims	Number Filed	Number Extra	RATE
Total Claims	33 - 20 =	13	X \$18.00 \$234.00
Independent Claims	4 - 3 =	1	X \$78.00 \$78.00
Multiple dependent claim(s) (if applicable)			+ \$260.00 \$0.00
TOTAL OF ABOVE CALCULATIONS = \$1002.00			
<p>Reduction by $\frac{1}{2}$ for filing by small entity, if applicable. Verified Small Entity Statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28)</p>			
SUBTOTAL = \$1152.00			
<p>Processing fee of \$130.00 for furnishing the English translation later than <u>20</u> <u>30</u> months from the earliest claimed priority date (37 CFR 1.492(f)).</p>			
<p>Extension of Time fee in the amount of \$</p>			
TOTAL NATIONAL FEE = \$1152.00			
<p>Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property</p>		<p>Amount to be refunded</p>	
TOTAL FEES ENCLOSED = \$1192.00			
		<p>Charged</p>	
<p>a. <input checked="" type="checkbox"/> A check in the amount of \$1192.00 to cover the above fees is enclosed.</p> <p>b. <input type="checkbox"/> Please charge my Deposit Account No. _____ in the amount of \$_____ to cover the above fees.</p> <p>c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-0089.</p>			
<p>NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.</p>			
<p>SEND ALL CORRESPONDENCE TO:</p> <p>Bruce H. Bernstein GREENBLUM & BERNSTEIN, P.L.C. 1941 Roland Clarke Place Reston, VA 20191 (703) 716-1191</p>			
<p> SIGNATURE Bruce H. Bernstein NAME</p>			
<p>29.027 REGISTRATION NUMBER</p>			

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Seiji SHIRAI et al.

Serial No : Not Yet Assigned (National Stage of PCT/JP99/00504

Filed : Concurrently Herewith

For : MULTILAYER PRINTED WIRING BOARD
WITH FILLED VIAHOLE STRUCTURE**PRELIMINARY AMENDMENT**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Prior to calculation of the filing fees and the examination of the above-identified patent application on the merits, the Examiner is respectfully requested to amend the claims as follows:

IN THE CLAIMS

Please cancel claim 34.

Please amend the claims as follows:

Claim 3, line 2, delete "or 2".

Claim 4, lines 1 and 2, change "any one of Claims 1 to 3" to ---Claim 1---.

Claim 5, lines 1 and 2, change "any one of Claims 1 to 4" to ---Claim 1---.

Claim 6, lines 1 and 2, change "any of Claims 1 to 5" to ---Claim 1---.

Claim 7, lines 1 and 2, change "any of Claims 1 to 6" to ---Claim 1---.

Claim 8, lines 1 and 2, change "any of Claims 1 to 7" to ---Claim 1---.

Claim 11, line 2, delete "or 10".

Claim 12, lines 1 and 2, change "any one of Claims 9 to 11" to ---Claim 9---.

Claim 13, lines 1 and 2, change "any one of Claims 9 to 12" to ---Claim 9---.

Claim 14, lines 1 and 2, change "any one of Claims 9 to 13" to ---Claim 9---.

Claim 15, lines 1 and 2, change "any of Claims 9 to 14" to ---Claim 9---.

Claim 16, lines 1 and 2, change "any of Claims 9 to 15" to ---Claim 9---.

Claim 19, lines 1 and 2, change "any Claims 17 or 18" to ---Claim 17---.

Claim 20, lines 1 and 2, change "any one of Claims 17 to 19" to ---Claim 17---.

Claim 21, lines 1 and 2, change "any of Claims 17 to 20" to ---Claim 17---.

Claim 22, lines 1 and 2, change "any of Claims 17 to 21" to ---Claim 17---.

Claim 23, lines 1 and 2, change "any of Claims 17 to 22" to ---Claim 17---.

Claim 24, lines 1 and 2, change "any of Claims 17 to 23" to ---Claim 17---.

Claim 27, line 2, delete "or 26".

Claim 28, lines 1 and 2, change "any of Claims 25 to 27" to ---Claim 25---.

Claim 29, lines 1 and 2, change "any one of Claims 25 to 28" to ---Claim 25---.

Claim 30, lines 1 and 2, change "any one of Claims 25 to 29" to ---Claim 25---.

Claim 31, lines 1 and 2, change "any one of Claims 25 to 30" to ---Claim 25---.

Claim 32, lines 1 and 2, change "any of Claims 25 to 31" to ---Claim 25---.

Claim 33, lines 1 and 2, change "any of Claims 25 to 32" to ---Claim 25---.

REMARKS

By the above amendment, claim 34 has been canceled to correspond to the Article 34 amendment in the PCT application and claims 3-8, 11-16, 19-24, and 27-33 have been amended to delete multiple dependency.

If there should be any questions, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,
Seiji SHIRAI et al.

Bruce H. Bernstein Reg. No. 29,027
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August 14, 2000
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SPECIFICATION

MULTILAYER PRINTED WIRING BOARD WITH FILLED VIAHOLE STRUCTURE

TECHNICAL FIELD

The present invention relates to a multilayer printed wiring board having a filled viahole structure, and more particularly to a multilayer printed wiring board adapted to assure an outstandingly secure adhesion between a conductor circuitry layer and an interlaminar insulative resin layer and form a fine conductor circuit pattern.

BACKGROUND ART

The multilayer printed wiring board includes a build-up multilayer printed wiring board in which conductor circuitry layers and insulative resin layers are alternately formed one on another and inner and outer ones of the conductor circuitry layers are electrically connected to each other by viaholes formed in the insulative resin layers. Generally, the viaholes in such a multilayer printed wiring board are formed by depositing a plating metal film on the inner wall and bottom of each of fine holes formed through the interlaminar insulative resin layers.

However, the multilayer printed wiring board having such viaholes formed through them are not advantageous in that the metal deposit is likely to break due to its precipitation or a heat cycle. To avoid this problem, it has recently been proposed to fill the viaholes with a plating metal (this structure will be referred to as "filled viahole structure" henceforth). Such filled viahole structures are known from the disclosure, for example, in the Japanese unexamined patent publication Nos. Hei 2-188992, Hei 3-3298 and Hei 7-34048.

The multilayer printed wiring board having the filled viahole structure is however disadvantageous in that a surface portion of the plating metal exposed outside the hole for viahole (the

surface will be referred to as "viahole surface" henceforth) is easily compressible. If an interlaminar resin insulating layer is formed on a conductor circuitry layer irrespectively of such a depression existent on the viahole surface, a corresponding depression will develop on the surface of the interlaminar insulative resin layer, and cause the plating metal film to break and also a trouble in mounting electronic parts on the wiring board.

The viahole surface where such a depression or concavity exists or is likely to exist can be flattened by applying an interlaminar resin more than once. However, the application of the interlaminar resin will lead to a greater thickness of the interlaminar insulative resin layer just above the depression on the viahole surface than that of the interlaminar insulative resin layer on the conductor circuitry layer. Thus in the process of forming a hole for a viahole in the interlaminar insulative resin layer by exposure, development and laser radiation, the interlaminar resin will partially remain inside the hole to lower the electrical connection reliability of the viahole. Especially for mass production of multilayer printed wiring boards, the residual resin is likely to occur since it is difficult to set different exposure and development conditions for the viahole surface from those for the conductor circuitry layer surface.

Further, to solve the problem of such a residual resin, a build-up multilayer printed wiring board has been proposed by the Japanese unexamined patent publication No. Hei 9-312472, etc.

In this conventional multilayer printed wiring board, a plating conductor or metal is filled in a hole for viahole so that a conductor circuitry layer has a thickness more than a half of the viahole diameter and thus the conductor circuitry

layer surface is at a same level as the viahole surface.

In this conventional multilayer printed wiring board, however, the inner wall of the hole formed in an interlaminar insulative resin layer should be plated with a thick layer of metal or conductor and thus a conductor circuitry layer formed along with the plating metal on the viahole will also be thick.

For a thicker plating, the plating resin should also be correspondingly thicker. As a result, light will be diffracted to inside a pattern on a photomasking film, so that the plating resist will be taper. That is, there will be resulted a conductor pattern which is thinner as it goes downward. Such a phenomenon will not matter so long as $L/S = 50/50 \mu\text{m}$ where L : line width; S : inter-line distance, but it will cause a pattern separation (peeling) if the pattern is a fine one of $L/S = 25/25 \mu\text{m}$.

Further, as disclosed in the Japanese unexamined patent publication No. Hei 2-188992, when a plating layer is formed and then it is etched to form a conductor circuitry layer, a thick plating layer will be undercut due to the etching and a fine pattern will be broken.

Furthermore, since in the filled viahole structure, a plating metal is filled in a hole for viahole, a larger stress will be caused by heat cycle than in a viahole formed just by plating an inner wall and bottom of a hole, so that a crack is likely to occur first in the viahole and then spread to an interlaminar insulative resin layer.

Moreover, an electroless plating method is used to fill the plating metal into the hole for viahole. However, the plating layer applied by the electroless plating is harder and less malleable than a one applied by the electroplating. Therefore, the plating layer is likely to crack under a thermal shock or due to heat cycle.

To solve the above problem, a method of forming a filled

viahole structure by using both electroless plating and electroplating has been proposed as disclosed in the Japanese unexamined patent publication No. Hei 9-312472.

In this filled viahole structure, however, the boundary between the electroless plating and electroplating layers is flat so that both the plating layers are separable from each other under a thermal shock or due to heat cycle. To avoid this separation, a plating resist has to be formed before a hole for viahole is filled with a metal by the electroplating. However, since the plating resist is formed on the electroless plating layer, the plating resist is easily separable and an inter-pattern shortcircuit will possibly take place.

Accordingly, the present invention has a primary object to overcome the above-mentioned drawbacks of the prior art by providing a multilayer printed wiring board having a filled viahole structure adapted to form a fine conductor circuit pattern and provide a highly reliable electrical connection between conductive circuitry layers.

The present invention has another object to provide a multilayer printed wiring board having a filled viahole structure adapted to assure a highly secure adhesion between a conductor circuitry layer and an interlaminar insulative resin layer and which will not crack even under a thermal shock or due to heat cycle.

DISCLOSURE OF THE INVENTION

The above objects can be attained by providing a multilayer printed wiring board worked out to meet some parameters the inventors' have found through various studies and under which there can be formed on a conductor layer between interlaminar insulative resin layers a conductor circuit pattern highly securely adhering to the interlaminar insulative resin layer and conductor layer.

According to one aspect of the present invention (henceforth, first embodiment), there is provided a build-up multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers having formed through them holes each filled with a plating layer to form a viahole, the surface of the plating layer exposed out of the hole for the viahole (the surface will be referred to as "viahole surface" henceforth) being formed substantially flat and lying at a substantially same level as the surface of the conductor circuit layer disposed in the interlaminar insulative resin layer in which the viahole also lies, and the thickness of the conductor circuitry layer being less than a half of the viahole diameter.

Note that the "viahole diameter" referred to herein means an opening diameter of the hole for the viahole.

The first embodiment having the above-mentioned filled viahole structure is advantageous as follows:

(1) Because no depression develops on the viahole surface, the surface of the interlaminar insulative resin layer is very flat, so a line breaking due to a depression hardly occurs and IC chips, etc. can be conveniently mounted on the wiring board.

(2) Since the thickness of the interlaminar insulative resin layer on the viahole and conductor circuitry layer is substantially uniform, the insulative resin of the interlaminar layer will less remain when a hole for the viahole is formed in the interlaminar insulative resin layer, thus the electrical connection by the viahole is more highly reliable.

(3) Since the thickness of the conductor circuitry layer is less than the half of the viahole diameter, it can be small although the hole for the viahole is filled with the plating metal. Thus the plating resin can be thin, which allows to form

a finer conductor circuit pattern.

According to another aspect of the present invention (henceforth, second embodiment), there is provided a build-up multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers having formed through them holes each filled with a plating layer to form a viahole, the thickness of the conductor circuitry layer being less than a half of the viahole diameter and less than 25 μm .

In the second embodiment having the above-mentioned filled viahole structure, the thickness of the plating conductor forming the conductor circuitry layer can be less than the half of the viahole and less than 25 μm . Thus, there can be formed a thinner plating resist having an improved resolution, which enables to easily form the conductor circuitry by etching and pattern an ultra-fine circuit.

The first and second embodiments of the present invention should preferably be constructed as follows:

① The viahole and conductor circuitry layer surfaces are roughened, which will contribute to an improved adhesion between the viahole, conductor circuitry layer and interlaminar insulative resin layers.

② The surface of the interlaminar insulative layer including the inner wall of the hole for the viahole is roughened. Thus, an improved adhesion is assured between the viahole formed from the filled plating metal and interlaminar insulative resin layer, as well as between the conductor circuitry layer and interlaminar insulative resin layer.

③ The conductor circuitry layer (inner pad) to which the viahole bottom connects has a surface thereof roughened and by which it is connected to the viahole. Thus, the adhesion

between the viahole and inner pad (inner conductor circuitry layer) is improved, which will lead to a possibility that the viahole and conductor circuitry layer is hardly separable from each other at their boundary even at a high temperature and humidity or by heat cycle.

Particularly, in a build-up multilayer printed wiring board derived from a combination of the above items ② and ③, the inner pad and also the viahole securely adhere to the interlaminar insulative resin layer, so that the inner pad and viahole are completely integral with each other with the interlaminar insulative resin layer lying between them.

④ The conductor circuitry layer has an edge thereof also roughened, which will prevent a crack which would take place first at the boundary between the conductor circuitry layer edge and interlaminar insulative resin layer due to an insufficient adhesion between the circuit edge and resin layer and spread the resin layer.

⑤ Preferably, another viahole should be formed on one viahole, which makes it possible to eliminate any dead space of the wiring by the viahole and thereby attain a further high density of wiring.

⑥ The interlaminar insulative resin layer should preferably be made of a composite of a thermoplastic resin and thermosetting resin or only a thermoplastic resin. Such a tough resin or resin compound filled in the viahole will be able to positively prevent a crack from taking place even when a great stress develops in the filled viahole.

⑦ The ratio between the viahole diameter and interlaminar insulative resin layer should preferably be within a range of 1 to 4, which will facilitate a finer patterning.

⑧ Particularly for the first embodiment, the thickness of the conductor circuitry layer of the first

embodiment should preferably be less than 25 μm . For easier formation of a fine pattern, the thickness should more preferably be 20 μm or less.

⑨ Especially for the second embodiment, the viahole surface exposed out of the hole for viahole, namely, the central portion of the exposed surface of the viahole should preferably be depressed and the depressed surface preferably be roughened.

The depression thus formed will provide an obtuse angle defined between contact surface edges of a viahole and a further viahole formed on the preceding one. A stress to the viahole surface edges is thus dispersed, so that a crack can be prevented from taking place and spreading from the contact surface edges to the interlaminar insulative resin layer.

The roughening of the depressed surface improves the adhesion between the viahole, conductor layer on which the conductor circuit is formed, and interlaminar insulative resin layer, which assures to prevent the conductor layer from separating from the other.

According to a still another aspect of the present invention (henceforth, third embodiment), there is provided a build-up multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers having formed through them holes each filled with a plating layer to form a viahole, the hole in the interlaminar insulative resin layer having at least an inner wall thereof roughened, the roughened inner wall of the hole being covered with an electroless plating layer, and an inner space of the hole defined by the electroless plating layer being filled with an electroplating layer to form the viahole.

In the third embodiment having the above-mentioned fill viahole structure, the electroless plating layer harder than

the electroplating layer is formed over the inner wall of the hole. The electroless plating layer bites, like anchor, the roughened surface, so it is not easily broken even if applied with a separating force.

As a result, the adhesion between the viahole and interlaminar insulative resin layer is improved. Also, since the electroplating layer having a larger malleability than the electroless plating layer fills the major part of the hole, the electroplating layer will flexibly follow the expansion and shrinkage of the interlaminar insulative resin layer, thus the layers can be prevented from being cracked under a thermal shock or due to heat cycle.

When the surface including the inner wall of the hole in the insulative resin layer is roughened, an electroless plating layer formed on the roughened surface will have a correspondingly roughened surface. The roughened surface or surface irregularity provides an effect of anchoring to assure a strong adhesion to the electroplating layer. Therefore, there will not occur any separation between the electroless plating layer and electroplating layer even under a thermal shock or due to heat cycle.

Also a plating resist applied on the roughened surface including the inner wall of the hole in the interlaminar insulative resin layer will have a close contact with the irregular surface of the electroless plating layer, and thus it will not easily be separated from the electroless plating layer surface. Therefore, there will not arise a shortcircuit between the conductor circuitry layers in the process of manufacturing a printed wiring board by the semi-additive method.

The third embodiment of the present invention should preferably be constructed as in the above items ① to ⑨.

According to a yet another aspect of the present invention

(henceforth, fourth embodiment), there is provided a build-up multilayer printed wiring board formed from conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers having formed through them holes each filled with a plating layer to form a via hole, the interlaminar insulative resin layer being formed from a composite of a fluororesin and a heat-resistant thermoplastic resin, composite of a fluororesin and a thermosetting resin, or a composite of a thermosetting resin and a heat-resistant thermoplastic resin.

In the fourth embodiment having the above-mentioned filled via hole structure, since the interlaminar insulative resin layer through which the via hole is provided is formed from a "composite of fluororesin and heat-resistant thermoplastic resin", "composite of fluororesin and thermosetting resin", or a "composite of thermosetting resin and heat-resistant thermoplastic resin", the metal layer will not crack first at the via hole even when the metal layer is expanded due to heat cycle. Also, the low dielectric constant of the fluororesin will not cause any delayed signal propagation.

The interlaminar insulative resin layer in the build-up multilayer printed wiring board according to the present invention should particularly preferably be formed from a composite of a cloth of fluororesin fiber and a thermosetting resin filled in voids in the cloth.

Also, the fourth embodiments should preferably be constructed as in the above-mentioned items ① to ④ and ⑥ to ⑧.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(a)-1(f) show various steps included in the process of manufacturing the first example of multilayer printed wiring board according to the present invention;

Figs. 2(a)-2(c) show further steps included in the process of manufacturing the first example of multilayer printed wiring board according to the present invention;

Figs. 3(a)-3(e) show various steps included in the process of manufacturing the eighth example of multilayer printed wiring board according to the present invention;

Figs. 4(a)-(4c) show further steps included in the process of manufacturing the eighth example of multilayer printed wiring board according to the present invention; and

Figs. 5(a) and 5(b) shows various steps included in the process of manufacturing the eleventh example of multilayer printed wiring board according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The best modes of carrying out the present invention will be discussed in detail with reference to the accompanying drawings.

(A) In a multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another and in which the interlaminar insulative resin layers have formed through them holes each filled with a plating layer to form a via hole, according to the first embodiment of the present invention, the surface of the via hole formed from each hole filled with the plating layer is formed substantially flat and lies at a substantially same level as the surface of the conductor circuit later disposed in the interlaminar insulative resin layer in which the via hole also lies, and the thickness of the conductor circuitry layer is less than a half of the via hole diameter.

In the printed wiring board according to the first embodiment, since the via hole surface is not depressed and so the surface of the interlaminar insulative resin layer is very flat, a line breaking due to a depression can be avoided, and IC chips, etc.

can be easily mounted on the wiring board without any inconvenience. Also, the interlaminar insulative resin layer on the viahole and conductive circuitry layer is uniformly thick, the resin will less reside when a hole for viahole is formed in the resin layer. Further, since the thickness of the conductor circuitry layer is less than the half of the viahole diameter, even when the hole for the viahole is filled with the plating metal to form a viahole, the conductor circuitry layer will have an increased thickness, so the plating resin layer can be thin, which allows to form a finer conductor circuit pattern.

In the multilayer printed wiring board having the above-mentioned filled viahole structure, the inner wall of the hole in the interlaminar insulative resin layer should preferably be roughened, which will improve the adhesion between the viahole formed from a filled plating metal and the interlaminar insulative resin layer.

Further, the viahole should preferably be connected to the roughened surface of the inner conductor circuitry layer. Since the roughened surface improve the contact and thus adhesion between the circuitry layer and viahole, the circuitry layer and viahole will not easily be separated from each other at their boundary even at a high temperature and humidity or by heat cycle.

Roughening the conductor circuitry layer, if applied, will advantageously prevent a crack which would develop first at the boundary between the circuitry layer and interlaminar insulative resin layer and then perpendicularly towards the interlaminar insulative resin layer.

The circuitry layer surface roughening should preferably be limited to a depth of 1 to 10 μm . A deeper surface roughening will cause an inter-layer short circuit while a shallower surface roughening will degrade the inter-layer adhesion.

The roughening should preferably be done by oxidation

(blackening), and reduction, of the surface of the circuitry layer, spraying an aqueous mixed solution of an organic acid and a cupric complex, or by electroless copper-nickel-phosphorus plating.

Of the above methods, the oxidation (blackening) and reduction use an oxidation bath of NaOH (20 g/l), NaClO₂ (50 g/l) and Na₃PO₄ (15.0 g/l), and a reduction bath of NaOH (2.7 g/l) and NaBH₄ (1.0 g/l), respectively.

In the spraying, the aqueous mixed solution of organic acid and cupric complex will dissolve a metal foil such as copper forming the lower conductor circuitry layer in the existence of oxygen, namely, during spraying or bubbling as will be discussed below:



where A : Complexing agent; n : Coordination number.

The cupric secondary complex used in the above method should preferably be a cupric secondary complex of any one of azoles. The cupric secondary complex of an azole is used to oxidize a metal copper. One should preferably be diazole, triazole or tetrazole, and more preferably, imidazole, 2-methylimidazole, 2-ethylimidazole, 2-ethyl-4-methylimidazole, 2-phenylimidazole or 2-undecylimidazole.

The cupric secondary complex of azole should preferably be used in an amount of 1 to 15 % by weight. In this range of content, the cupric secondary complex shows an outstanding solubility and stability.

The organic acid is used in the aqueous solution to dissolve the copper oxide, and should preferably be at least one selected from formic acid, acetic acid, propionic acid, butyric acid, valeric acid, caproic acid, acrylic acid, crotonic acid, oxalic acid, malonic acid, succinic acid, glutaric acid, maleic

acid, benzoic acid, glycolic acid, lactic acid, malic acid, and sulfamic acid.

The content of the organic acid should preferably be 0.1 to 30 % by weight in order to maintain the solubility of the copper oxide and stability of the dissolved copper oxide.

Acuprous complex produced will be dissolved under the action of the acid and combined with an oxygen to produce a cupric secondary complex which will contribute to copper oxidation again.

To promote oxidation of copper dissolution and azole oxidation, a halogen, for example, fluorine ion, chlorine ion or bromine ion may be added to an etchant or etching solution of the organic acid and cupric complex. The halogen ion may be one to which hydrochloric acid, sodium chloride, etc. is added.

The content of the halogen ion should preferably be 0.01 to 20 % by weight. In this range of content, the layer surface roughened by attacking by the etchant will provide a secure adhesion between the conductor circuitry layer and interlaminar insulative resin layer.

The etchant of the organic acid and cupric secondary complex is prepared by dissolving a cupric secondary complex of an azole and an organic acid (containing a halogen ion as necessary) in water.

For the formation of a needle-like alloy by the electroless copper-nickel-phosphorus plating, a plating bath should preferably be used which is composed of 1 to 40 g/l of copper sulfate, 0.1 to 6.0 g/l of nickel sulfate, 10 to 20 g/l of citric acid, 10 to 100 g/l of hypophosphite, 10 to 40 g/l of boric acid and 0.01 to 10 g/l of a surfactant.

Further, in the multilayer printed wiring board according to this embodiment, a further via hole should preferably be formed on one filled via hole to eliminate any via hole-caused dead space

for wiring, which will implement a higher density of wiring.

According to this embodiment, the multilayer printed wiring board can use, as the interlaminar insulative resin layer, a thermosetting resin, thermoplastic resin, or a composite of thermosetting and thermoplastic resins.

More preferably for this embodiment, the interlaminar insulative resin layer should be formed from a composite of thermosetting and thermoplastic resins.

The thermosetting resin may be a one selected from epoxy resin, polyimide resin, phenol resin, thermosetting polyphenylether (PPE), etc.

The thermoplastic resin may be a one selected from fluororesins such as polytetrafluoroethylene (PTFE), polyethylene terephthalate (PET), polysulfone (PSF), polyphenylene sulfide (PPS), thermoplastic polyphenylene ether (PPE), polyether sulfone (PES), polyether imide (PEI), polyphenylene sulfone (PPES), tetrafluoroethylene hexafluoropropylene copolymer(FEP) , tetra fluoroethylene perfluoroalcoxy copolymer (PFA), polyethylene naphthalate (PEN), polyether ether ketone (PEEK), polyolefin, etc.

The composite of thermosetting and thermoplastic resins may be a composite of epoxy resin with PES, PSF, PPS or PPES, or similar.

This embodiment should preferably use a composite of a fluororesin fiber cloth and a thermosetting resin charged in voids in the cloth since the composite shows a low dielectric constant and high dimensional stability.

In this case, the thermosetting resin should preferably be at least a one selected from epoxy resin, polyimide resin, polyamide resin and phenol resin.

The fluororesin fabric cloth should preferably be a texture or nonwoven fabric made from the fluororesin fibers. The

nonwoven fabric is produced by forming a sheet from short or long fluororesin fibers and a binder and heating the sheet to fuse the fibers to each other.

Also, this embodiment of the present invention can use an adhesive for use in the electroless plating as the interlaminar insulative resin layer.

The electroless plating adhesive should optimally be prepared by dispersing cured heat-resistant resin particles soluble in acid or oxidizing agent into a non-cured heat-resistant resin which will be made insoluble in acid or oxidizing agent by curing. This electroless plating adhesive is most suitably usable because the heat-resistant resin particles can be dissolved and removed in the presence of an acid or oxidant to have formed thereon a roughened surface which can securely anchor an adjoining layer.

The electroless plating adhesive, namely, the cured heat-resistant resin particles, should preferably be at least a one selected from a heat-resistant resin powder of 10 μm or less in mean particle size, agglomerate produced by coagulating heat-resistant resin particles of 2 μm or less in mean particle size, mixture of a heat-resistant resin powder of 2 to 10 μm or less in mean particle size and a heat-resistant resin powder of 2 μm or less in mean particle size, dummy particles produced by depositing at least a one selected from a heat-resistant resin powder or inorganic powder of 2 μm or less in mean particle size on the surface of a heat-resistant resin powder of 2 to 10 μm in mean particle size, mixture of a heat-resistant resin powder of 0.1 to 0.8 μm in mean particle size and a heat-resistant resin powder of over 0.8 μm and under 2 μm in mean particle size, and a heat-resistant resin powder of 0.1 to 1.0 μm in mean particle size. This electroless plating adhesive can be used to form a more complicated anchoring surface.

The heat-resistant resin used in the electroless plating adhesive may be any one of the aforementioned thermosetting resin, thermoplastic resin and composite of thermosetting and thermoplastic resins. Particularly, the composite of thermosetting and thermoplastic resins is optimally usable for this embodiment of the present invention.

The multilayer printed wiring board according to the first embodiment of the present invention has been described in the foregoing. This printed wiring board is manufactured as will be described herebelow with reference to FIGS. 1 and 2.

(1) First, a wiring substrate is prepared by forming on either side of a core substrate 1 an inner conductor circuit pattern 2 (as in FIG. 1(a)).

The core substrate 1 is a laminate coppered on either side thereof. The inner conductor circuit pattern 2 is formed by etching the copper layer on either side of the core substrate 1. Alternatively, the core substrate 1 may be a glass epoxy substrate, polyimide substrate, ceramic substrate, or a metal substrate. In this case, the inner conductor pattern 2 is provided on the core substrate 1 by forming an electroless plating adhesive layer on the core substrate 1, roughening the adhesive layer surface and by plating the roughened surface with a metal by the electroless plating method. Otherwise, the inner conductor pattern 2 is provided on the core substrate 1 by the semi-additive method. More particularly, the entire roughened surface of the electroless plating adhesive layer is electroless-plated, a plating resist is applied selectively on the roughened surface, a surface portion not applied with the plating resist is electroplated, then the plating resist is removed, and the entire surface is etched, thereby producing the conductor circuit pattern 2 consisting of electroplating and electroless plating layers.

Further, a layer 3 having a roughed surface is formed as necessary on the surface of the inner conductor circuit pattern 2 on the wiring substrate as shown in FIG. 1(b). The roughed surface layer 3 is made of copper, nickel and phosphorus.

The roughed surface layer 3 is formed by electroless plating. The aqueous electroless plating solution should preferably have a copper ion concentration of 2.2×10^{-2} to 4.1×10^{-2} mol/l, nickel ion concentration of 2.2×10^{-3} to 4.1×10^{-3} mol/l and a hypophosphorus ion concentration of 0.20 to 0.25 mol/l.

A layer thus precipitated from the electroplating solution will have a needle crystalline structure which provide an excellent anchorage. In the electroless plating solution, a complex and additive may be added to the above-mentioned compound.

The surface of the layer 3 is roughened by an electroless copper-nickel-phosphorus plating, oxidizing and reducing, etching the copper surface along the grain boundary, or otherwise, as described in the above.

Note that the core substrate 1 has formed therein through-holes through which the inner conductor circuit patterns 2 on the opposite sides of the core substrate 1 are electrically connected to each other.

Also the through-holes and spaces between the conductor circuit patterns 2 may be filled with a resin to assure a surface flatness.

(2) Next, an interlaminar insulative resin layer 4 is formed on either side of the wiring substrate prepared at the above step (1) (as in FIG. 1(c)).

Particularly, for the first embodiment of the present invention, the interlaminar insulative resin layer 4 in which viaholes 9 are to be formed as will further be discussed later should preferably be an electroless plating adhesive containing

as resin matrix a composite of a thermosetting resin and thermoplastic resin.

(3) After the interlaminar insulative resin layer or electroless plating adhesive layer 4 formed at the above step (2) is dried, holes 5 for the viaholes are formed in the layer 4 (as in FIG. 1(d)).

In case the resin of the interlaminar insulative layer 4 is a photosensitive one, the hole 5 is formed by exposing, developing and then thermally curing the layer 4. When the resin is a thermosetting one, the hole 5 is formed by thermally curing the layer 4 and then Laser drilling. At this time, the ratio D/T_1 between the viahole diameter (D) and interlaminar insulative resin layer thickness (T_1) should preferably be within a range of 1 to 4. This is because if the ratio D/T_1 is less than 1, the electroplating solution will not enter the hole while the ratio over 4 will not allow the hole to be filled with a plating metal sufficiently.

(4) Next, the epoxy resin particles existent on the surface of the cured adhesive layer 4 are removed by decomposing or dissolving with an acid or oxidant to rough the surface of the adhesive layer 4. Thus a roughened or rough surface 6 is formed. (Also see FIG. 1(e).)

The acid used for this purpose should preferably be a one selected from phosphoric acid, hydrochloric acid, sulfuric acid and an organic acid such as formic acid or acetic acid. It should more preferably be an organic acid for it will not attack a metallic conductor layer exposed out of the viahole when the surface of the adhesive layer 4 is roughened.

The oxidant should preferably be chromic acid, or permanganic acid (such as potassium permanganate).

(5) Next, a catalyst nucleus is applied to the roughened surface 6 of the adhesive layer 4.

The catalyst nucleus should preferably be a precious metal ion or colloid. Generally, it is a palladium chloride or palladium colloid. More preferably, it should be a palladium. To fix the catalyst nucleus, it is heated.

(6) Further, the roughened surface 6 of the electroless plating adhesive layer 4 is electroless plated to form an electroless plating layer 7 of which the surface is correspondingly rough to the roughened surface 6 (as in FIG. 1(f)). The electroless plating layer 7 should be 0.1 to 5 μm thick, and more preferably 0.5 to 3 μm .

Next, a plating resist layer 8 is formed on the electroless plating layer 7 (as in FIG. 2(a)). The plating resist should preferably be composed of an acrylate of a cresol novolac type epoxy resin or phenol novolac type epoxy resin, and an imidazole curing agent. It may a commercially available dry film.

(7) Further, a surface portion of the electroless plating layer 7 on which the plating resist layer is not formed is electroplated to form a conductor layer on which an upper conductor circuit 12 is to be formed, and an electroplating layer 9 is filled in the hole 5 to form a viahole 10 (as in FIG. 2(b)). At this time, the electroplating layer 9 exposed out of the hole 5 should preferably be 5 to 30 μm thick so that the upper conductor circuit 12 will have a thickness T_2 not exceeding a half of the diameter D of the viahole ($T_2 < D/2$).

For the electroplating, copper plating should preferably be used.

(8) Furthermore, the plating resist layer 8 is removed, and then the electroless plating layer under the plating resist is dissolved and removed in a mixed solution of sulfuric acid and hydrogen peroxide or an etchant of sodium persulfate or ammonium persulfate to provide an independent upper conductor circuitry layer 12 and filled viahole 10.

(9) Next, the surface of the upper conductor circuitry layer 12 is roughened to form a roughened surface 14.

The roughened surface 14 may be formed by etching, polishing, oxidizing and reducing, or plating.

First for oxidation and reduction, respectively, an oxidation bath is prepared from 20 g/l of NaOH, 50 g/l of NaClO₂ and 15.0 g/l of NaPO₄ and a reduction bath is prepared from 2.7 g/l of NaOH and 1.0 g/l of NaBH₄.

If the roughed surface layer 14 is made of an alloy of copper-nickel-phosphorus, the alloy is precipitated by an electroless plating.

As an electroless plating solution for this alloy, a reduction bath should preferably be used which is composed of 1 to 40 g/l of copper sulfate, 0.1 to 6.0 g/l of nickel sulfate, 10 to 20 g/l of citric acid, 10 to 100 g/l of hypophosphite, 10 to 40 g/l of boric acid and 0.01 to 10 g/l of surfactant.

Further, the rough surface layer 14 is covered with a layer of a metal or a precious metal of which the ionization tendency is larger than that of copper and smaller than that of titanium.

For covering the roughened surface layer 14 with tin, a solution of tin boronfluoride and thiocarbamide, or a solution of tin chloride and thiocarbamide, should be used. In this case, an Sn layer of 0.1 to 2 μm or so in thickness is formed as a result of Cu-Sn substitution.

For covering the roughened surface layer 14 with a precious metal, spattering or evaporation may be adopted.

(10) Next, an electroless plating adhesive layer 16 is formed, as an interlaminar insulative resin layer, on the wiring substrate having been processed.

(11) Further, the steps (3) to (8) are repeated to provide a further viahole 20 just on the viahole 10 and a further upper conductor circuitry layer 22 above the upper conductor circuit

12. The surface of the further via hole 20 is formed as a conductor pad which functions as a solder pad.

(12) Next, a solder resist composition is applied to the outer surface of the wiring substrate having been processed as in the foregoing. After the solder resist layer is dried, a photomasking film having a hole pattern depicted thereon is placed on the solder resist layer. The solder resist layer is exposed and developed to form holes in which the solder pad portion (including conductor pad and via hole) of the conductor layer is exposed. The opening diameter of the exposed hole may be larger than the diameter of the solder pad so that the solder pad will be exposed. Alternatively, the opening diameter of the hole may be smaller than the diameter of the solder pad so that the edge of the solder pad will be covered with the solder resist layer. In the latter case, the solder pad can be retained under the solder resist layer, and thus it can be prevented from being separated.

(13) Next, metal layers of "nickel and gold", respectively, are formed on the solder pad exposed out of the hole.

The nickel layer should preferably be 1 to 7 μm thick, and the gold layer be 0.01 to 0.06 μm thick for a thicker nickel layer will increase the resistance while a smaller thickness of the nickel layer will render itself easily separable. Concerning the gold layer, a larger thickness will lead to an increased manufacturing cost while a smaller thickness will lower the adhesion to the solder layer.

(14) Next, a solder is fed onto the solder pad exposed out of the hole to produce a 6-layered printed wiring board. The solder is fed by the solder transfer or printing method.

In the solder transfer method, a solder foil is attached to a prepreg, and the solder foil is etched with only a portion

thereof corresponding to the hole to form a solder pattern which will be a solder carrier film. After a flux is applied to the hole in the solder resist on the substrate, the solder carrier film is attached on the flux and heated to transfer the solder.

On the other hand, in the solder printing method, a printing mask (metallic) having through-holes formed in positions corresponding to the solder pads is placed on the wiring substrate and a solder paste is printed on the mask and heated.

In the printed wiring board according to the first embodiment, a solder bump is formed on the filled viahole. In the conventional printed wiring board, since the viahole is not filled, a larger amount of solder paste is required to form a solder bump as high as a solder bump of a flat solder pad. Namely, the hole in the printing mask has to be large. According to this embodiment of the present invention, however, since the viahole is filled, the solder paste may be applied in a uniform amount and the holes in the printing mask may have a same size.

(B) Next, the second embodiment of the present invention will further be discussed herebelow. In a multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers having formed through them holes each filled with a plating layer to form a viahole, according to the second embodiment, the thickness of the conductor circuitry layer is less than a half of the viahole diameter and less than 25 μm .

In the filled viahole structure of the printed wiring board according to the second embodiment, the thickness of the plating conductor forming the conductor circuitry layer can be less than the half of the viahole and less than 25 μm . Thus, there can be formed a thinner plating resist having an improved resolution, which makes it possible to easily form the conductor circuitry

layer by etching and pattern an ultra-fine circuit.

Further, since the conductor circuitry layer has the thickness less than the half of the opening diameter of the via hole and less than 25 μm , the area of contact of the edge of the conductor circuitry layer with the interlaminar insulative resin layer is reduced correspondingly. Therefore, the central portion of the via hole surface should preferably be depressed and roughened, whereby the adhesion between the conductor layer and interlaminar insulative resin layer can be improved and thus separation between them can be prevented. More specifically, a stress developed due to heat cycle can be dispersed so that the conductor and insulative layers can be prevented from being separated from each other.

The aforementioned second embodiment should preferably be constructed as will be described herebelow:

① The filled via hole and inner conductor circuitry layer (inner pad) are electrically connected to each other by a roughened surface layer provided on the surface of the inner conductor circuitry layer to improve the adhesion between the via hole and inner conductor circuit.

② The filled via hole and conductor circuitry layer has their surfaces roughened to improve the adhesion between them and the outer interlaminar insulative resin layer.

③ The conductor circuitry layer has also an edge thereof roughened.

④ The roughened surface layer on the surface of the conductor circuitry layer is 1 to 10 μm thick.

⑤ The surface roughing is done as in the first embodiment.

⑥ A further via hole is formed on the filled via hole.

⑦ The surface including the inner wall of the interlaminar insulative resin layer is roughened.

⑧ The interlaminar insulative resin layer is made of a thermosetting resin, thermoplastic resin, or a composite of thermosetting and thermoplastic resins, and preferably of the composite of thermosetting and thermoplastic resins or the thermoplastic resin.

The thermosetting resin, thermoplastic resin and composite of thermosetting and thermoplastic resins may be selected from those having previously been described concerning the first embodiment, and so they will not be discussed any longer.

Next, the multilayer printed wiring board having the aforementioned filled viahole structure according to the second embodiment are manufactured as will be described below with reference to FIGS. 1 and 2.

The manufacturing process is substantially same as that for the first embodiment and thus includes the previously mentioned steps (1) to (14).

At the step (7), when electroplating the portion not applied with the plating resist with a conductor layer which will form a conductor circuit, and filling a plating layer into the hole to form the viahole, the electroplating layer should preferably be formed to a thickness of 5 to 20 μm so that the conductor circuitry layer has a thickness less than a half of the viahole diameter and less than 25 μm .

(C) Next, the third embodiment of the present invention will be described. In a multilayer printed wiring board formed from conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers having formed through them holes each filled with a plating layer to form a viahole, according to the third embodiment, the inner wall of the hole formed in the interlaminar insulative resin layer is roughened, the roughened inner wall of the hole is covered with a roughened electroless

plating layer, and an inner space of the hole defined by the electroless plating layer is filled with an electroplating layer.

In the filled via hole structure of the multilayer printed wiring board according to the third embodiment, the electroless plating layer harder than the electroplating layer is formed over the inner wall of the hole. The electroless plating layer bites, like anchor, the roughened surface, so it is not easily broken even when a separating force is applied, and the adhesion between the via hole and interlaminar insulative resin layer is improved. Also, since the electroplating layer having a larger malleability than the electroless plating layer fills the major part of the hole, the electroplating layer will flexibly follow the expansion and shrinkage of the interlaminar insulative resin layer, thus the layers can be prevented from being cracked under a thermal shock or due to heat cycle.

Since the inner wall of the hole in the interlaminar insulative resin layer is roughened, there is provided an improved adhesion between the via hole and interlaminar insulative resin layer. The electroless plating layer formed on the roughened surface is so thin as to follow the irregularity of the roughened surface. This surface irregularity serves as anchor to provide a strong adhesion to an electroplating layer. Therefore, the electroless plating layer and electroplating layer will not be separated from each other even due to heat cycle or under a thermal shock.

Other surface than the hole inner wall is also roughened, the roughened surface is electroless plated, and further a plating resist is applied to the electroless plating layer. The plating resist applied on the roughened surface will closely adhere to the irregular surface of the electroless plating layer, and thus it will not easily be separated from the electroless plating layer surface. Therefore, there will not arise a short circuit

between the conductor circuitry layers in the process of manufacturing the printed wiring board by the semi-additive method.

The electroless plating layer forming the above-mentioned conductor circuit should preferably be 0.1 to 5 μm , and more preferably 1 to 5 μm for a thickness too larger than 5 μm will not assure to sufficiently follow the shape of the roughened surface of the interlaminar insulative resin layer while a thickness too smaller than 1 μm will lower the separating or peeling strength and cause a large resistance which will interfere with a subsequent electroplating, so that the plating layer thickness will not be uniform.

The electroplating layer forming the conductor circuit should preferably have a thickness within a range of 5 to 30 μm , and more preferably a thickness ranging from 10 to 20 μm . This is because a larger thickness will cause the peeling strength to be lower while a smaller thickness will increase the resistance, so that the electroplating will result in an uneven precipitation.

Next, the multilayer printed wiring board having the aforementioned filled viahole structure according to the third embodiment is manufactured as will be discussed herebelow with reference to FIGS. 1 and 2.

The manufacturing process is substantially same as that for the first embodiment and thus includes the previously mentioned steps (1) to (14).

At the step (7) among others, when electroplating the portion not applied with the plating resist with a conductor layer which will form a conductor circuit, and filling a plating layer into the hole to form the viahole, the electroplating layer should preferably be 5 to 20 μm thick so that the conductor circuitry layer is less than a half of the viahole diameter.

Further according to this embodiment, the plating solution composition, plating temperature, dipping length of time and agitating conditions should preferably be controlled to depress the central portion of the plating layer exposed out of the hole that forms the viahole. The depression should preferably have a size less than the thickness of the conductor layer, and more preferably be 20 μm or less. This is because a bigger depression will result in a larger thickness of the interlaminar insulative resin layer formed on the depression than that of the resin layer formed on the other conductor layers. When the resin layer is exposed, developed and lased, it is likely to partially remain on the depression in the viahole, which will lower the electrical connection reliability of the viahole.

(D) Next, the fourth embodiment of the present invention will further be discussed herebelow. In a multilayer printed wiring board formed from conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers having formed through them holes each filled with a plating layer to form a viahole, according to the fourth embodiment, the interlaminar insulative resin layer is formed from a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin, or a composite of thermosetting resin and heat-resistant resin.

In the filled viahole structure of the fourth embodiment discussed above, the interlaminar insulative resin layer in which the viahole is provided is formed from a highly tough composite of fluororesin and heat-resistant thermoplastic resin, or a highly tough composite of fluororesin and thermosetting resin. So, even if the viahole is made from a hole filled with a plating layer, since the metal layer is thermally expanded during heat cycle, no crack will develop first at the viahole. Also, the

fluororesin has so low a dielectric constant that signal will be propagated with no delay.

In this embodiment, the interlaminar insulative resin layer in which the viahole is formed should preferably be formed from a composite of fluororesin and heat-resistant thermoplastic resin, or a composite of fluororesin and thermosetting resin.

The fluororesin should preferably be a polytetrafluoroethylene since it is a most versatile fluororesin.

The heat-resistant thermoplastic resin should preferably be a one which can be thermally decomposed at a temperature higher than 250°C and that is selected from fluororesins such as polytetrafluoroethylene (PTFE), polyethylene terephthalate (PET), polysulfone (PSF), polyphenylene sulfide (PPS), thermoplastic polyphenylene ether (PPE), polyether sulfone (PES), polyether imide (PEI), polyphenylene sulfone (PPES), tetrafluoroethylene hexafluoropropylene copolymer (FEP), tetrafluoroethylene perfluoroalcoxy copolymer (PFA), polyethylene naphthalate (PEN), polyether ether ketone (PEEK), polyolefin, etc.

The thermosetting resin may be epoxy resin, polyimide resin, phenol resin, thermosetting polyphenylene ether (PPE), or similar.

The composite of fluororesin and thermosetting resin should preferably be a composite of fluororesin fabric cloth and thermosetting resin charged in voids in the cloth.

In this case, the a fluororesin fabric cloth should preferably be a texture or nonwoven fabric made from the fluororesin fibers. The nonwoven fabric is produced by forming a sheet from short or long fluororesin fibers and a binder and heating the sheet to fuse the fibers to each other.

Further, the thermosetting resin should preferably be at

least a one selected from epoxy resin, polyimide resin, polyamide resin and phenol resin. The composite of thermosetting and thermoplastic resins may be a composite of epoxy resin with PES, PSF, PPS or PPES, or similar.

The multilayer printed wiring board according to the fourth embodiment is manufactured as will be described herebelow with reference to FIGS. 3 and 4.

The manufacturing process is substantially same as that for the first embodiment and thus includes the previously mentioned steps (1) to (14).

At the step (2), a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin or a composite of thermosetting and thermoplastic resins is used as the interlaminar insulative resin layer. Particularly, an electroless plating adhesive using the composite as resin matrix should preferably be used.

At the step (3), after the electroless plating adhesive is dried, holes for the viaholes are formed in the layer.

In case the interlaminar insulative layer is made of a resin photosensitized by acrylating, the hole for the viahole is formed by exposing, developing and then thermally curing the resin layer. When the resin is a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin or a composite of thermosetting and thermoplastic resins, the hole for the viahole is formed by thermosetting the resin layer and then by lasing drilling. At this time, the ratio D/T_1 between the viahole diameter (D) and interlaminar insulative resin layer thickness (T_1) should preferably be within a range of 1 to 4. This is because if the ratio D/T_1 is less than 1, the electroplating solution will not enter the hole while the ratio over 4 will not allow the hole to sufficiently be filled with a plating metal.

Further at the step (4), the surface of the interlaminar insulative resin layer should preferably be roughened by plasma etching or the like for this roughening will improve the adhesion to the plating layer.

In case an electroless plating adhesive is used as the interlaminar insulative resin layer, the epoxy resin particles existent on the surface of the cured adhesive layer are removed by decomposing or dissolving with an acid or oxidant to rough the surface of the adhesive layer.

Examples:

To confirm the advantages of the aforementioned first to fourth preferred embodiments of the present invention, examples 1 to 9 and comparative examples 1 to 8 of multilayer printed wiring boards were prepared through the steps (1) to (11) of the 14 steps having been described in the foregoing, not yet including the step at which the solder bump is formed. Example 11 was prepared through all the steps (1) to (14). The multilayer printed wiring boards thus prepared will further be described in detail herebelow:

Example 1:

(1) Compositions prepared through the following steps ① to ③ were mixed together and agitated to prepare an electroless plating adhesive.

① Thirty-five parts by weight of a 25% acrylated product of cresol novolac type epoxy resin (80% in solid content; 250 in molecular weight, by Nippon Kayaku Co., Ltd.), 4 parts by weight of photosensitive monomer (ARONIX M315 by Toa Gosei Co., Ltd.), 0.5 part by weight of antifoaming agent (S-65 by SANNOPCO) and 3.6 parts by weight of NMP, were mixed by agitation.

② Eight parts by weight of polyether sulfone (PES) and 7.245 parts by weight of epoxy resin particles (POLYMERPOE by Sanyo Kasei Co., Ltd.) of 0.5 μm in mean particle size were

mixed together and then 20 parts by weight of NMP were added to the mixture. They were mixed by agitation.

③ Two parts by weight of imidazole curing agent (2E4MZ-CN by Shikoku Kasei Co., Ltd.), 2 parts by weight of initiator (IRGACURE I-907 by Ciba Geigy), 0.2 part by weight of photosensitizer (DETX-S by Nippon Kayaku Co., Ltd.) and 1.5 parts by weight of NMP were mixed together by agitation.

(2) A substrate 1 made of bismaleimide triazine (BT) and having a conductor circuitry layer 2 formed on either surface thereof (as in FIG. 1(a)) was dipped in an electroless plating solution composed of 8 g/l of copper sulfide, 0.6 g/l of nickel sulfide, 15 g/l of citric acid, 29 g/l of sodium hypophosphite, 31 g/l of boric acid and 0.1 g/l of surfactant and having a pH of 9 to precipitate a roughened surface layer 3 of copper, nickel and phosphorus to a thickness of 3 μm on the surface of the conductor circuitry layer 2. Then, the substrate 1 was washed in water. It was dipped in an electroless tin-substitution plating bath composed of 0.1 mol/l of tin boron-fluoride and 1.0 mol/l of thiocarbamide at 50°C for 1 hour to precipitate a tin layer of 0.3 μm on the surface of the roughened surface layer 3 (as in FIG. 1(b); the tin layer is not illustrated).

(3) The interlaminar insulative resin layer prepared at the above step (1) was applied to the substrate 1 (see FIG. 1(c)). After the substrate 1 was dried, a photomasking film was placed on the substrate 1, exposed, developed and thermally cured to form a 20 μm -thick interlaminar insulative resin layer 4 having formed through them holes 5 for viaholes of which the diameter is 60 μm (61 μm at bottom and 67 μm at top) (see FIG. 1(d)).

(4) The substrate 1 having the interlaminar insulative resin layer 4 formed thereon was dipped in chromic acid for 19 min to form a roughed surface layer 6 of 4 μm in depth on the surface of the layer 4 (see FIG. 1(e)).

(5) The substrate 1 having the rough surface layer 6 formed thereon was dipped in an electroless plating solution to form an electroless plating layer 7 of 0.6 μm in thickness over the rough surface (see FIG. 1(f)).

(6) A plating resist layer 8 was formed on the electroless plating layer 7 in the conventional manner (see FIG. 2(a)).

(7) Next, a portion on which the plating resist layer 8 was not formed was electroplated under the following conditions to form an electroplating layer 9 of 20 μm in thickness on the portion. The layer 9 provided a conductor layer on which a conductor circuit 12 was to be formed, and the electroplating layer 9 was filled in the hole to form a viahole 10 (as in FIG. 2(b)).

Aqueous electroplating solution:

$\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$	60 g/l
Leveling agent (HL by ATOTTECH)	40 ml/l
Sulfuric acid	190 g/l
Brightening agent (UV by ATOTTECH)	0.5 ml/l
Chlorine ion	40 ppm

Electroplating conditions:

Bubbling	3.0 liters/min
Current density	0.5 A/dm ²
Set current value	0.18 A
Plating length of time	130 min

(8) The plating resist layer 8 was separated and removed, and then the electroless plating layer 7 under the plating resist layer 8 was dissolved for removal in an etching solution composed of a mixture of sulfuric acid and hydrogen peroxide, sodium persulfate, ammonium persulfate, etc. to form the conductor circuit 12 consisting of the electroless plating layer 7 and electroplating copper layer 9 and of which the thickness is about 20 μm and L/S ratio is 25/25 μm . At this time, the viahole 10 had a flat surface and the conductor circuit surface and viahole

surface were at a same level.

The inventors of the present invention found that when the thickness T of the interlaminar insulative resin layer 4 was 20 μm while the viaholes 10 were formed to have diameters D of 25, 40, 60 and 80 μm , the plating layers required for filling the viaholes 10 were 10.2, 11.7, 14.8 and 23.8 μm thick, respectively.

(9) As at the step (2), a roughened surface layer 3 was formed on the substrate. Further, the steps (3) to (8) were repeated to produce a multilayer printed wiring board (as in FIG. 2(c)).

Example 2:

A multilayer printed wiring board was prepared in the same manner as the aforementioned example 1 except that an interlaminar insulative resin layer was formed by attaching a fluororesin film of 20 μm in thickness to the layer by thermo-compression bonding and holes for viaholes of 60 μm in diameter were formed by irradiating ultraviolet laser.

Example 3:

(1) A drawn tetrafluoroethylene resin (PTFE) fiber available as fiber for woven fabric from the W. L. Gore & Associates, Inc. (trade name: GORE-TEX) was used to weave a cloth for an interlaminar insulative resin layer. The cloth was composed of 53 fibers of 400 deniers per 2.54 cm in longitudinal direction and 52 fibers of 400 deniers per 2.54 cm in lateral direction.

(2) The fluororesin fiber cloth was cut to a sheet of 15.24 cm by 15.24 cm, and the cloth sheet was immersed in a solution of alkaline metal and naphthalene available under the trade name TETRA-ETCH from the W. L. Gore & Associates. After that, the cloth sheet was washed in warm water to rinse away the acetone. The fibers appeared dark brown due to the etching and the cloth shrank 20% in both longitudinal and lateral directions. The cloth sheet was stretched to the initial dimensions with the

edges thereof held in hands.

On the other hand, a liquid epoxy resin was prepared as a thermosetting resin which was to be impregnated into the fluororesin fiber cloth according to the guide line stated in the Dow Chemical's Products Catalog No. 296-396-783 for Dowepoxy resin products 521-A80.

(3) The liquid epoxy resin was impregnated into the fluororesin fiber cloth prepared at the above step (2). The fluororesin fiber cloth impregnated with the epoxy resin was dried at 160°C to provide a B-stage sheet. The sheet was 0.3556 cm in thickness and the impregnated resin in the sheet weighed 5 g.

(4) The B-stage sheet was attached on the substrate at the step (2) for the example 1, and pressed under a pressure of 80 kg/cm² at 175°C to form an interlaminar insulative resin layer. Further, the layer was exposed to an ultraviolet laser of 220 nm in wavelength to form holes for viaholes of 60 µm in diameter. Thereafter, the steps (4) to (9) for the example 1 was repeated to produce a multilayer printed wiring board.

Comparative example 1:

As disclosed in the Japanese unexamined patent publication No. Hei 2-188992, a multilayer printed wiring board was produced in the same manner as the aforementioned example 1 except that a conductor circuit was made only of an electroless plating layer of 25 µm in thickness and viaholes were formed by dipping for 11 hours in an electroless plating aqueous solution composed of 0.06 mol/l of copper sulfide, 0.3 mol/l of formalin, 0.35 mol/l of NaOH, 0.35 mol/l of EDTA and a small amount of additive at 75°C and having a pH of 12.4.

In the wiring board, the holes in the interlaminar insulative resin layer were found filled with the plating layer, but a depression of 20 to 25 µm was found in the central portion of

the plating layer.

Comparative example 2:

According to the disclosure in the Japanese unexamined patent publication No. Hei 2-312472, a multilayer printed wiring board was produced. More particularly, the steps (1) to (5) for the embodiment 1 were repeated to process a substrate and then the substrate was dipped in an electroless plating solution prepared from an aqueous solution composed of 0.05 mol/l of copper sulfide, 0.30 mol/l of formalin, 0.35 mol/l of sodium hydroxide, and 0.35 mol/l of ethylenediaminetetraacetic acid (EDTA) to form a plating layer of 40 μm in thickness.

Further, a dry film was attached to the substrate, exposed and developed to form an etching resist of $L/S = 25/25 \mu\text{m}$ on the substrate. For etching, the substrate was dipped in a mixed solution of sulfuric acid and hydrogen peroxide. However, the conductor circuitry layer was undercut and separated. Therefore, the comparative example 2 was not evaluated.

The examples 1 to 3 and comparative example 1 were evaluated as to ① surface flatness of their interlaminar insulative resin layer and ② electrical connection reliability of the viahole.

The above item ①, surface flatness, was evaluated by judging whether a depression developed on a first applied interlaminar insulative resin layer. The item ②, electrical connection reliability of the viahole, was evaluated by checking, using a probe, whether a further viahole formed on a viahole already formed showed a poor electrical continuity. The evaluation results are shown in Table 1.

As seen from Table 1, the examples 1, 2 and 3 are superior in surface flatness of the interlaminar insulative resin layer. Even when the further viahole is provided on the inner one, a circuit pattern breaking due to a depression is not observed, namely, the examples

Table 1

	Depression on interlaminar insulitative resin layer	Poor electrical continuity
Example 1	No	No
Example 2	-	No
Example 3	-	No
Comparative example 1	Yes	No

1 to 3 have a high electrical connection reliability of the via hole, and IC chip and other devices can easily be mounted on the wiring boards with no inconvenience. Further, even when mass-produced, the examples 1 to 3 will show a high electrical connection reliability of the via holes.

Owing to the structure of the examples 1 to 3, a fine circuit pattern of $L/S = 25/25 \mu\text{m}$ can be formed.

As mentioned above, the first embodiment of the present invention provides a multilayer printed wiring board having a filled via hole structure enabling a fine circuit pattern to be formed and showing superior surface flatness and high electrical connection reliability of the via hole.

Example 4:

A multilayer printed wiring board was produced by repeating the steps (1) to (5) for the example 1, and further processing the substrate as follows:

(6) A plating resist layer 8 of $15 \mu\text{m}$ in thickness and $L/S = 25/25 \mu\text{m}$ was formed on the electroless plating layer 7 in the conventional manner (see FIG. 2(a)).

(7) Next, a portion on which the plating resist layer 8 was not formed was electroplated under the following conditions to form an electroplating layer $15 \mu\text{m}$ in thickness on the portion. The layer 9 provided a conductor layer on which a conductor circuit was to be formed, and the electroplating layer 9 was filled in the hole to form a via hole 10 (as in FIG. 2(b)).

Aqueous electroplating solution:

<chem>CuSO4.5H2O</chem>	60 g/l
Leveling agent (HL by ATOTTECH)	40 ml/l
Sulfuric acid	190 g/l
Brightening agent (UV by ATOTTECH)	0.5 ml/l
Chlorine ion	40 ppm

Electroplating conditions:

Bubbling	3.0 liters/min
Current density	0.5 A/dm ²
Set current value	0.18 A
Plating length of time	100 min

(8) The plating resist layer 8 was separated and removed, and then the electroless plating layer 7 under the plating resist layer 8 was dissolved for removal in an etching solution composed of a mixture of sulfuric acid and hydrogen peroxide, sodium persulfate, ammonium persulfate, etc. to form a conductor circuit 11 from the electroless plating layer 7 and electroplating copper layer 9 and having a thickness of about 15 μm and L/S ratio of 25/25 μm . At this time, the viahole 10 had a depression of about 5 μm in depth found on the surface hereof.

(9) As at the step (2) for the example 1, a rough surface layer 3 was formed on the substrate. Further, the steps (3) to (8) for the example 1 were repeated to produce a multilayer printed wiring board (as in FIG. 2(c)).

Owing to the depression formed on the central surface portion of the viahole, the thin conductor layer was not separable so that a fine circuit pattern of L/S = 25/25 μm could be positively formed.

Example 5:

A multilayer printed wiring board was produced by repeating the steps (1) to (3) for the example 3, and further processing the substrate as follows:

(4) The B-stage sheet was attached on the substrate at the step (2) for the example 4, and pressed under a pressure of 80 kg/cm² at 175°C to form an interlaminar insulative resin layer. Further, the layer was exposed to an ultraviolet laser of 220 nm in wavelength to form holes for viaholes of 60 µm in diameter. Thereafter, the steps (4) to (9) for the example 4 was repeated to produce the multilayer printed wiring board.

Comparative example 3:

A multilayer printed wiring board was produced similarly to the embodiment 1 as disclosed in the Japanese unexamined patent publication No. Hei 2-188992. As a result, the holes in the interlaminar insulative resin layer were found filled with the plating layer. For a circuit pattern of L/S = 25/25 µm, however, the plating resist was etched but too much, resulting in breakage of the circuit pattern.

Comparative example 4:

According to the Japanese unexamined patent publication No. Hei 9-312472, a multilayer printed wiring board was produced. More particularly, the steps (1) to (5) for the embodiment 5 were repeated and then the substrate was dipped in an electroless plating solution prepared from an aqueous solution composed of 0.05 mol/l of copper sulfide, 0.30 mol/l of formalin, 0.35 mol/l of sodium hydroxide, and 0.35 mol/l of ethylenediaminetetraacetic acid (EDTA) to form a plating layer of 40 µm in thickness.

A dry film was attached to the substrate, exposed and developed to form an etching resist of L/S = 25/25 µm on the substrate. For etching, the substrate was dipped in a mixed solution of sulfuric acid and hydrogen peroxide. However, the conductor circuitry layer was undercut and separated.

As having been described in the above, the second embodiment of the present invention provides a multilayer printed wiring

board having a filled viahole structure which can surely prevent the wiring board from line-breakage and implement an ultrafine circuit pattern of L/S = 25/25 μm .

Example 6:

A multilayer printed wiring board was produced by repeating the steps (1) to (5) for the example 1, and further processing the substrate as follows:

(6) A plating resist layer 8 of 15 μm in thickness and L/S = 25/25 μm was formed on the electroless plating layer 7 in the conventional manner (see FIG. 2(a)).

(7) Next, a portion on which the plating resist layer 8 was not formed was electroplated under the following conditions to form an electroplating layer 15 μm in thickness on the portion. The layer 9 provided a conductor layer on which a conductor circuit was to be formed, and the electroplating layer 9 was filled in the hole to form a viahole 10 (as in FIG. 2(b)).

Aqueous electroplating solution:

$\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$	60 g/l
Leveling agent (HL by ATOTTECH)	40 ml/l
Sulfuric acid	190 g/l
Brightening agent (UV by ATOTTECH)	0.5 ml/l
Chlorine ion	40 ppm

Electroplating conditions:

Bubbling	3.0 liters/min
Current density	0.5 A/dm ²
Set current value	0.18 A
Plating length of time	100 min

(8) The plating resist layer 8 was separated and removed, and then the electroless plating layer 7 under the plating resist layer 8 was dissolved for removal in an etching solution composed of a mixture of sulfuric acid and hydrogen peroxide, sodium persulfate, ammonium persulfate, etc. to form a conductor circuit

11 made of the electroless plating layer 7 and electroplating copper layer 9 and having a thickness of about 15 μm and L/S ratio of 25/25 μm . At this time, the via hole 10 had a flat surface.

(9) As at the step (2) for the example 1, a rough surface layer 3 was formed on the substrate. Further, the steps (3) to (8) for the example 1 were repeated to produce a multilayer printed wiring board (as in FIG. 2(c)).

Owing to the depression formed on the central surface portion of the via hole, the thin conductor layer was not separable so that a fine circuit pattern of L/S = 25/25 μm could be formed.

Example 7:

A multilayer printed wiring board was produced by repeating the steps (1) to (3) for the example 2, and further processing the substrate as follows:

(4) The B-stage sheet was attached on the substrate at the step (2) for the example 6, and pressed under a pressure of 80 kg/cm^2 at 175°C to form an interlaminar insulative resin layer. Further, the layer was exposed to an ultraviolet laser of 220 nm in wavelength to form holes for via holes of 60 μm in diameter. Thereafter, the steps (4) to (9) for the example 6 was repeated to produce the multilayer printed wiring board.

Comparative example 5:

A multilayer printed wiring board was produced similarly to the embodiment as disclosed in the Japanese unexamined patent publication No. hei 2-188992. In this case, the holes for via holes were filled only with the electroless plating layer to form the via holes.

Comparative example 6:

A multilayer printed wiring board was produced by repeating the steps (1) to (3) for the example 6 and further processing the substrate as follows. The substrate was dipped in an electroless plating solution prepared from an aqueous solution

composed of 0.05 mol/l of copper sulfide, 0.30 mol/l of formalin, 0.35 mol/l of sodium hydroxide, and 0.35 mol/l of ethylenediaminetetraacetic acid (EDTA) to form a plating layer of 1 μm in thickness.

Further the steps (6) to (9) for the example 6 were repeated to produce the multilayer printed wiring board.

Note that this multilayer printed wiring board had no roughed surface on the viahole.

For checking a separation and crack at the viahole, the examples 6 and 7 and comparative examples 5 and 6 were heated at 128°C for 48 hours, and then heated and cooled alternately 1,000 times at a temperature ranging from -55°C to 125°C. The test results are shown in Table 2.

Table 2

	Separation of viahole	Cracking in viahole
Example 6	No	No
Example 7	No	No
Comparative example 5	No	Yes
Comparative example 6	Yes	No

As seen from Table 2, the comparative example 5 showed a cracking in the viahole portion, and the comparative example 6 showed a separation of the viahole portion. However, the examples 6 and 7 showed neither separation nor cracking at the viahole portion.

As having been described in the foregoing, the third embodiment of the present invention provides a multilayer printed wiring board having a filled viahole structure in which the viahole is not easily separable and no crack takes place under a thermal shock or due to heat cycle.

Example 8:

A multilayer printed wiring board was produced of which the

interlaminar insulative resin layer was made of a composite of fluororesin and heat-resistant thermoplastic resin, through a process including the following steps:

(1) An interlaminar insulative resin liquid was prepared by thermally fusing and mixing eight parts by weight of polyether sulfone (PES) and 92 parts by weight of fluororesin (Teflon by Du Pont) at 350°C.

(2) A substrate 1 made of bismaleimide triazine (BT) and having a conductor circuitry layer 2 formed on either surface thereof (as in FIG. 3(a)) was dipped in an electroless plating solution composed of 8 g/l of copper sulfide, 0.6 g/l of nickel sulfide, 15 g/l of citric acid, 29 g/l of sodium hypophosphite, 31 g/l of boric acid and 0.1 g/l of surfactant and having a pH of 9 to precipitate a roughened surface layer 3 of copper, nickel and phosphorus to a thickness of 3 μm on the surface of the conductor circuitry layer 2. Then, the substrate 1 was washed in water. It was dipped in an electroless tin-substitution plating bath composed of 0.1 mol/l of tin boron-fluoride and 1.0 mol/l of thiocarbamide at 50°C for 1 hour to precipitate a tin layer of 0.3 μm on the surface of the roughened surface layer 3 (as in FIG. 1(b); the tin layer is not illustrated).

(3) The interlaminar insulative resin liquid prepared at the above step (1) was applied to the substrate 1 processed at the step (2) (as in FIG. 3(c)), and cooled to form an interlaminar insulative resin layer 4 of 20 μm in thickness. An ultraviolet laser of 220 nm in wavelength was irradiated to the interlaminar insulative resin layer 4 to form holes 5 of 60 μm in diameter for viaholes (as in FIG. 3(d)).

(4) Using Pd as target, sputtering was made at 200 W for 1 min to implant Pd nucleus into the interlaminar insulative resin layer 4.

(5) The substrate 1 processed at the step (4) was dipped

in the electroless plating solution to form an electroless plating copper layer 7 to a thickness of 0.6 μm over the surface of the interlaminar insulative resin layer 4 including the holes (as in FIG. 3(e)).

(6) A plating resist layer 8 was formed on the electroless plating copper layer 7 in the conventional manner (see FIG. 4(a)).

(7) Next, a portion on which the plating resist layer 8 was not formed was electroplated under the following conditions to form an electroplating layer of 15 μm in thickness on the portion. The layer 9 provided a conductor layer on which a conductor circuit was to be formed, and the electroplating layer 9 was filled in the hole to form a viahole 10 (as in FIG. 4(b)).

Aqueous electroplating solution:

<chem>CuSO4.5H2O</chem>	60 g/l
Leveling agent (HL by ATOTTECH)	40 ml/l
Sulfuric acid	190 g/l
Brightening agent (UV by ATOTTECH)	0.5 ml/l
Chlorine ion	40 ppm

Electroplating conditions:

Bubbling	3.0 liters/min
Current density	0.5 A/dm ²
Set current value	0.18 A
Plating length of time	130 min

(8) The plating resist layer 8 was separated and removed, and then the electroless plating copper layer 7 under the plating resist layer 8 was dissolved for removal in an etching solution composed of a mixture of sulfuric acid and hydrogen peroxide, sodium persulfate, ammonium persulfate, etc. to form a conductor circuit 11 from the electroless plating copper layer 7 and electroplating copper layer 9 and having a thickness of about 15 μm .

At this time, the viahole 10 had a flat surface, and the

conductor circuitry layer surface was at a same level as the viahole surface.

(9) As at the step (2), a rough surface layer 3 was formed on the substrate. Further, the steps (3) to (8) were repeated to produce the multilayer printed wiring board (as in FIG. 4(c)).

Example 9:

A multilayer printed wiring board was produced of which the interlaminar insulative resin layer was made of a composite of fluororesin and thermosetting resin, by repeating the above steps (1) to (3) for the example 3 and further processing the substrate as follows:

(4) The B-stage sheet was attached on the substrate at the step (2) for the example 8, and pressed under a pressure of 80 kg/cm² at 175°C to form an interlaminar insulative resin layer. Further, the layer was exposed to an ultraviolet laser of 220 nm in wavelength to form holes for viaholes of 60 µm in diameter. Thereafter, the steps (4) to (9) for the example 8 was repeated to produce the multilayer printed wiring board.

Example 10:

A multilayer printed wiring board of which the interlaminar insulative resin layer was made of a composite of thermosetting and thermoplastic resins was produced by repeating the steps (1) to (6) for the example 1 and further processing the substrate as follows:

(7) A portion on which the plating resist layer was not formed was electroplated under the same conditions as at the step (7) for the example 8 to form an electroplating layer 15 µm in thickness on the portion. The layer 9 provided a conductor layer on which a conductor circuit was to be formed, and the electroplating layer 9 was filled in the hole to form a viahole 10.

(8) The plating resist layer 8 was separated and removed, and then the electroless plating layer 7 under the plating resist

layer 8 was dissolved for removal in an etching solution composed of a mixture of sulfuric acid and hydrogen peroxide, sodium persulfate, ammoniumpersulfate, etc. to form a conductor circuit 11 having a thickness of about 15 μm and consisting of the electroless plating layer 7 and electroplating copper layer 9.

At this time, the viahole 10 had a flat surface, and the conductor surface was at a same level as the viahole surface.

(9) As at the step (2), a rough surface layer was formed on the substrate. Further, the steps (3) to (8) were repeated to produce the multilayer printed wiring board.

Comparative example 7:

A multilayer printed wiring board was produced of which the interlaminar insulative resin layer was made only of a thermosetting resin, as follows:

(1) Compositions prepared through the following steps ① to ③were mixed together and agitated to prepare an electroless plating adhesive.

① Thirty-five parts by weight (80% in solid content) of a 25% acrylated product of cresol novolac type epoxy resin (2500 in molecular weight, by Nippon Kayaku Co., Ltd.), 4 parts by weight of photosensitive monomer (ARONIX M315 by Toa Gosei Co., Ltd.), 0.5 part by weight of antifoaming agent (S-65 by SANNOPCO) and 3.6 parts by weight of NMP, were mixed by agitation.

② Twenty parts by weight of NMP were added to 7.245 parts by weight of epoxy resin particles (POLYMERPOLE by Sanyo Kasei Co., Ltd.) of 0.5 μm in mean particle size. They were mixed together by agitation.

③ Two parts by weight of imidazole curing agent (2E4MZ-CN by Shikoku Kasei Co., Ltd.), 2 parts by weight of initiator (IRGACURE I-907 by Ciba Geigy), 0.2 part by weight of photosensitizer (DETX-S by Nippon Kayaku Co., Ltd.) and 1.5 parts by weight of NMP were mixed together by agitation.

Thereafter, steps (2) to (9) for the example 10 were repeated to provide the multilayer printed wiring board.

Comparative example 8:

A multilayer printed wiring board was produced in the same manner as for the example 8 except that no leveling agent and brightening agent were added to the electroplating solution. As a result, a plating layer could not sufficiently be filled in the holes for the viaholes.

For evaluation of the examples 8 to 10 and comparative examples 7 and 8, they were subjected to a heat cycle test in which they were heated and cooled alternately 500 times at a temperature ranging from -55°C to 125°C, and then to another heat cycle in which they were heated and cooled alternately 1,000 times at the temperature range of -55°C to 125°C. A light-optic microscope was used to check for any crack having started at the viahole, separation or crack of the plating layer forming the viahole. The test results are shown in Table 3.

Table 3

	Crack starting at viahole		Separation or crack of plating layer	
	500 heat cycles	1000 heat cycles	500 heat cycles	1000 heat cycles
Example 8	No	No	No	No
Example 9	No	No	No	No
Example 10	No	Yes	No	No
Comparative example 7	Yes	Yes	No	No
Comparative example 8	No	No	Yes	Yes

As seen from Table 3, the example 8 is highly resistant against violent temperature variation since its interlaminar insulative resin layer incorporates a fluororesin and thermoplastic resin.

As having been described in the foregoing, the fourth embodiment of the present invention provides a multilayer printed

wiring board having a filled viahole structure permitting to positively prevent line breakage in the wiring board and improved in resistance against violent temperature variation.

Example 11:

A multilayer printed wiring board was produced by repeating the steps (1) to (9) for the example 1, and further processing the substrate as follows:

(10) As at the step (2) for the example 1, a roughened surface layer 3 was provided by electroless copper- nickel-phosphorus plating.

On the other hand, a solder resist composition was prepared by mixing 46.67 parts by weight of a photosensitive oligomer (4000 in molecular weight) produced by acrylating 50% of epoxy group of a 60% by weight of cresol novolac type epoxy resin (by Nippon Kayaku Co., Ltd.) solved in DMDG (diethyleneglycoldimethylether), 6.666 parts by weight of a 80% by weight of bisphenol A type epoxy resin (EPICOAT 1001 by YUKA SHELL) solved in MEK (methyletylketone), 6.666 parts by weight of an epoxy resin of the same bisphenol A type (EPICOATE-1001-B80 by YUKA SHELL), 1.6 parts by weight of imidazole (2E4MZ-CN by Shikoku Kasei Co., Ltd.), 1.5 parts by weight of a polyvalent acryl monomer being a photosensitive monomer (R604 by Nippon Kayaku Co., Ltd.), 3.0 parts by weight of a same polyfunctional acryl monomer (DPE6A by KYOEISHA KAGAKU Co., Ltd.) and 0.36 part by weight of leveling agent made from an acrylic ester polymer (POLYFLOW No. 75 by KYOEISHA KAGAKU). Further, 2.0 parts by weight of an initiator (IRGACURE I-907 by Ciba Geigy) and 0.2 part by weight of photosensitizer (DETX-S (by Nippon Kayaku Co., Ltd.) were added to the above mixture. Furthermore, 0.6 part by weight of DMDG was added to the mixture to adjust the viscosity to 1.4 ± 0.3 Pa·s at 25°C.

The viscosity of the solder resist composition was measured

using a B-type viscometer (DVL-B by Tokyo Keiki). For 60 rpm, No. 4 rotor was used with the viscometer. For 6 rpm, No. 3 rotor was used.

(11) The substrate prepared at the step (10) was applied on either side thereof with the solder resist composition to a thickness of 20 μm . The substrate was dried at 70°C for 20 min, and then at 70°C for 30 min. Then, a photomasking film of 5 mm in thickness having a circular pattern (mask pattern) depicted thereon was mounted on the substrate, and the substrate was exposed to an ultraviolet radiation of 1000 mJ/cm^2 in wavelength and developed in DMDG.

Further, the substrate was heated at 80°C for 1 hour, at 100°C for 1 hour, at 120°C for 1 hour and then at 150°C for 3 hours to form a solder resist layer 120 (of 20 μm in thickness) open at the solder pad portion thereof (opening diameter of 200 μm) (as in FIG. 5(a)).

(12) Next, the substrate having the solder resist layer 120 formed thereon was dipped for 20 min in an aqueous electroless plating solution composed of 30 g/l of nickel chloride, 10 g/l of sodium hypophosphite and 10 g/l of sodium citrate and having a pH of 5, to form a nickel plating layer 140 of 5 μm in thickness on the hole inner wall. Further, the substrate was dipped in an aqueous electroless plating solution composed of 2 g/l of gold potassium cyanide, 75 g/l of ammonium chloride, 50 g/l of sodium citrate and 10 g/l of sodium hypophosphite at 93°C for 23 sec to precipitate a gold plating layer 150 to a thickness of 0.03 μm on the nickel plating layer 140.

(13) A printing mask was placed on the hole in the solder resist layer 120, a solder paste was printed and reflowed at 200°C to form a solder bump (solder) 160. Thus a printed wiring board having the solder bump was produced (as in FIG. 5(b)).

In the conventional printed wiring board, since the viahole

is not filled, a large amount of solder paste has to be used or the printing mask hole has to be large to form a solder bump as high as the solder bump of a flat solder pad. In the multilayer printed wiring board according to the present invention, however, since the via hole is filled, the solder paste can be applied uniformly and the hole in the printing mask may be uniform in size.

INDUSTRIAL APPLICABILITY

As having been described in the foregoing, the present invention provides a multilayer printed wiring board best suitable for forming a fine circuit pattern thereon, providing an excellent adhesion between the conductor circuit and interlaminar insulative resin layer and an outstanding resistance against cracking due to heat cycle.

Therefore, the multilayer printed wiring board according to the present invention has an excellent applicability in many fields of art requiring a high performance and high packaging density of electronic parts.

CLAIMS

1. A multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through them holes each filled with a plating layer to form a viahole, characterized by:

the surface of said plating layer exposed out of the hole for the viahole being formed substantially flat and lying in a substantially same level as the surface of the conductor circuit layer disposed in the interlaminar insulative resin layer in which the plating layer also lies; and

the thickness of said conductor circuitry layer being less than a half of the viahole diameter.

2. The multilayer printed wiring board as set forth in Claim 1, wherein the inner wall of the hole is roughened.

3. The multilayer printed wiring board as set forth in Claim 1 or 2, wherein the plating layer surface and conductor circuit surface exposed out of the hole for the viahole are roughened.

4. The multilayer printed wiring board as set forth in any one of Claims 1 to 3, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

5. The multilayer printed wiring board as set forth in any one of Claims 1 to 4, wherein a further viahole is formed on the viahole.

6. The multilayer printed wiring board as set forth in any of Claims 1 to 5, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

7. The multilayer printed wiring board as set in any of Claims 1 to 6, wherein the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of

1 to 4.

8. The multilayer printed wiring board as set forth in any of Claims 1 to 7, wherein the conductor circuitry layer has a thickness less than 25 μm .

9. A multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through them holes each filled with a plating layer to form a viahole, characterized in that the thickness of said conductor circuitry layer is less than a half of the viahole diameter and less than 25 μm .

10. The multilayer printed wiring board as set forth in Claim 9, wherein the inner wall of the hole is roughened.

11. The multilayer printed wiring board as set forth in Claim 9 or 10, wherein a depression is formed on the central surface portion of the plating layer surface exposed out of the hole for the viahole.

12. The multilayer printed wiring board as set forth in any one of Claims 9 to 11, wherein the plating layer surface and conductor circuit surface exposed out of the hole for the viahole are roughened.

13. The multilayer printed wiring board as set forth in any one of Claims 9 to 12, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

14. The multilayer printed wiring board as set forth in any one of Claims 9 to 13, wherein a further viahole is formed on the viahole.

15. The multilayer printed wiring board as set forth in any of Claims 9 to 14, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

16. The multilayer printed wiring board as set in any of Claims 9 to 15, wherein the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of 1 to 4.

17. A multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through them holes each filled with a plating layer to form a viahole, characterized by:

 said hole having an inner wall thereof roughened;

 said roughened inner wall being covered with a roughened electroless plating layer; and

 an inner space of said hole defined by the electroless plating layer and filled with an electroplating layer.

18. The multilayer printed wiring board as set forth in Claim 17, wherein depressions are formed in the central surface portion of the plating layer surface exposed out of the hole for the viahole.

19. The multilayer printed wiring board as set forth in any Claim 17 or 18, wherein the plating layer surface and conductor circuit surface exposed out of the hole for the viahole are roughened.

20. The multilayer printed wiring board as set forth in any one of Claims 17 to 19, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

21. The multilayer printed wiring board as set forth in any one of Claims 17 to 20, wherein a further viahole is formed on the viahole.

22. The multilayer printed wiring board as set forth in any of Claims 17 to 21, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic

resin or a composite of thermoplastic and thermosetting resins.

23. The multilayer printed wiring board as set in any of Claims 17 to 22, wherein the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of 1 to 4.

24. The multilayer printed wiring board as set forth in any of Claims 17 to 23, wherein the conductor circuitry layer has a thickness less than 25 μm .

25. A multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through them holes each filled with a plating layer to form a viahole, characterized by:

 said interlaminar insulative resin layer being formed from a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin, or a composite of thermosetting resin and heat-resistant thermoplastic resin.

26. The multilayer printed wiring board as set forth in Claim 25, wherein the interlaminar insulative resin layer is made of a composite of fluororesin fiber cloth and thermosetting resin impregnated in the voids in the cloth.

27. The multilayer printed wiring board as set forth in Claim 25 or 26, wherein the inner wall of the hole is roughened.

28. The multilayer printed wiring board as set forth in any of Claims 25 to 27, wherein depressions are formed in the central surface portion of the plating layer surface exposed out of the hole for the viahole.

29. The multilayer printed wiring board as set forth in any one of Claims 25 to 28, wherein the plating layer surface and conductor circuit surface exposed out of the hole for the viahole

are roughened.

30. The multilayer printed wiring board as set forth in any one of Claims 25 to 29, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

31. The multilayer printed wiring board as set forth in any one of Claims 25 to 30, wherein a further viahole is formed on the viahole.

32. The multilayer printed wiring board as set in any of Claims 25 to 31, wherein the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of 1 to 4.

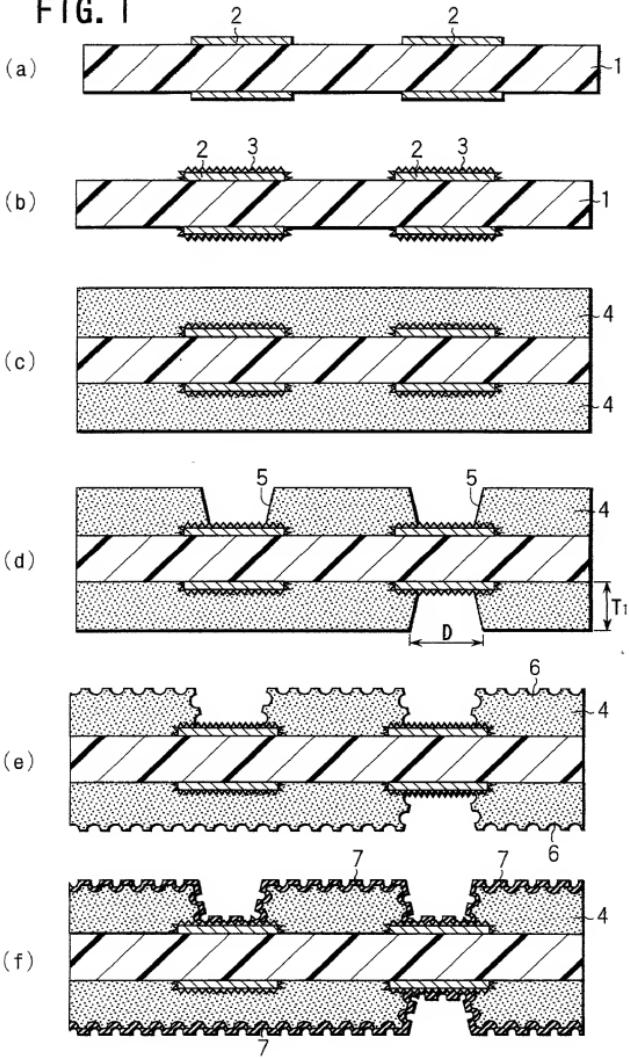
33. The multilayer printed wiring board as set forth in any of Claims 25 to 32, wherein the conductor circuitry layer has a thickness less than 25 μm .

34. (canceled)

ABSTRACT

The present invention provides a multilayer printed wiring board having a filled viahole structure advantageously usable for forming a fine circuit pattern thereon, and having an excellent resistance against cracking under a thermal shock or due to heat cycle. The multilayer printed wiring board is comprised of conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through them holes each filled with a plating layer to form a viahole. The surface of the plating layer exposed out of the hole for the viahole is formed substantially flat and lies at a substantially same level as the surface of the conductor circuit disposed in the interlaminar insulative resin layer. The thickness of the conductor circuitry layer is less than a half of the viahole diameter and less than 25 μm . The inner wall of the hole formed in the interlaminar insulative resin layer is roughened and an electroless plating layer is deposited on the roughened surface. An electroplating layer is filled in the hole including the electroless plating layer to form the viahole. The interlaminar insulative resin layer is formed from a composite of a fluororesin showing a high fracture toughness and a heat-resistant thermoplastic resin, a composite of fluororesin and thermosetting resin or a composite of thermosetting and thermoplastic resins.

FIG. 1



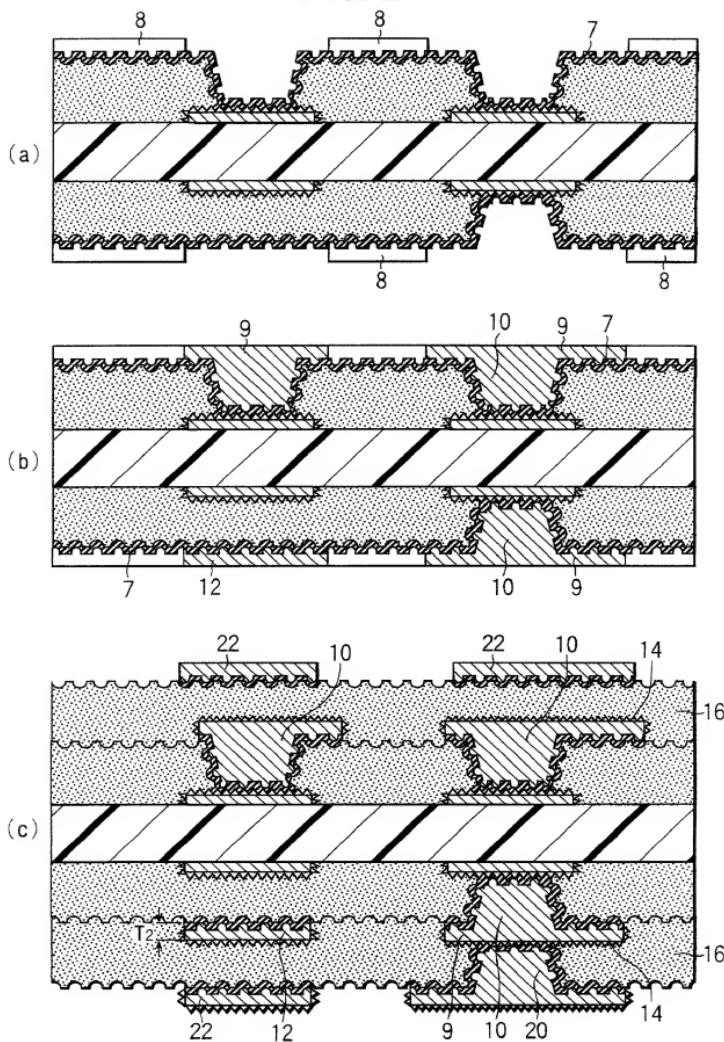
2/5
FIG. 2

FIG. 3

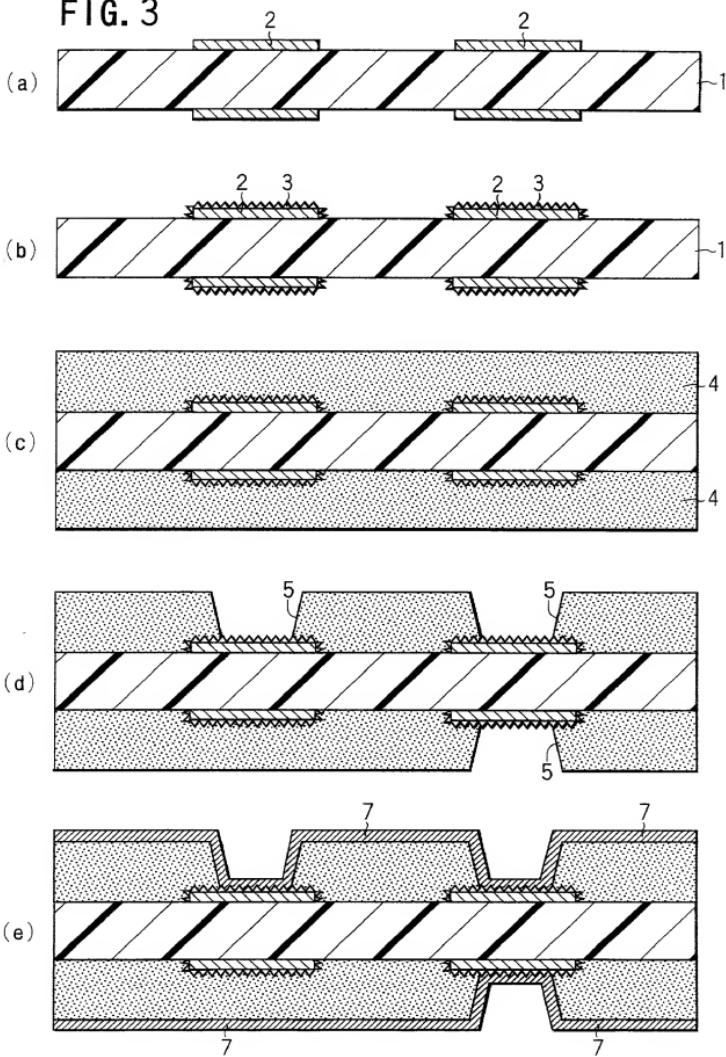
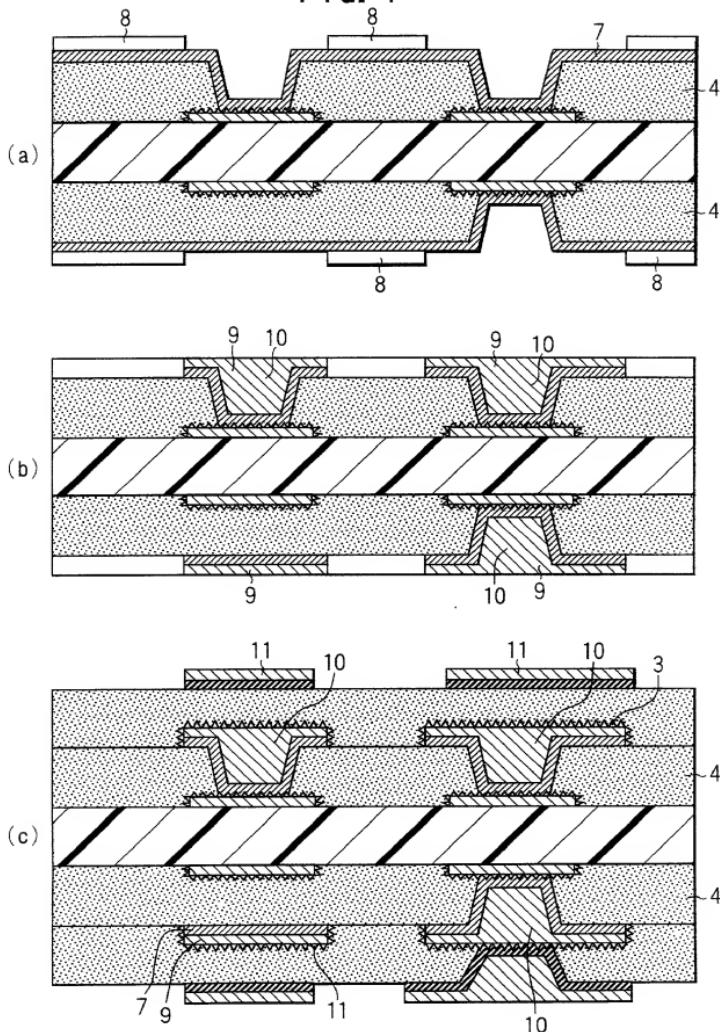
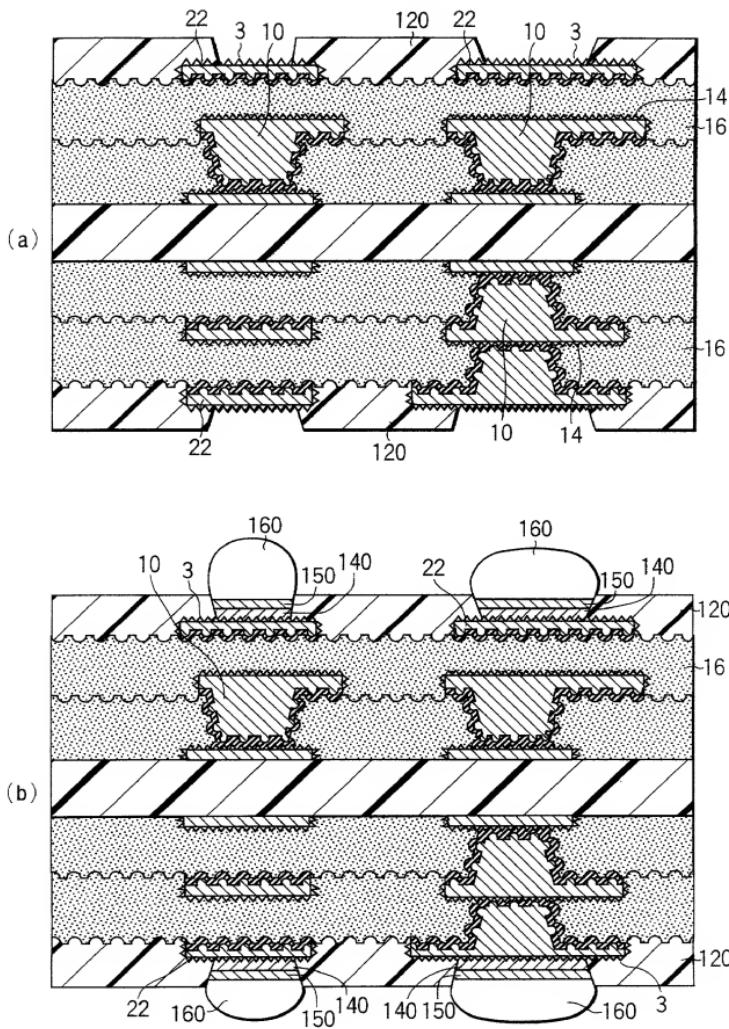


FIG. 4



5/5

FIG. 5



Declaration and Power of Attorney For Utility or Design Patent Application

特許出願宣言書

Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のとおり

宣言する：

私の住所、郵便の宛先および国籍は、下欄に氏名に統一して記載したとおり
であり、

名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、
最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている
場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が
下欄に記載されている場合）と信じ、

上記発明の明細書（下記の欄でX印がついていない場合は、
本書に添付）は、

□ 年 月 日に提出され、
米国出願番号 とし、
(該当する場合) 年 月 日に訂正されました。又は、

特許協定条約出願番号 とし、
(該当する場合) 年 月 日に訂正されました。

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

私は、連邦規則法典第37編第1条第56項に定義されるとおり、特許資格の有無について重要な情報を顯示すべき義務があることを認めます。

私は合衆国法典第35部第119条(a-d)項又は第365条(b)項に基づく、下記の外国特許出願又は発明者証出願、或いは第365条(a)項に基づく、少なくとも米国以外の1ヶ国を指したPCT国際出願の外国優先権を主張し、更に優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願、又は発明者証出願あるいはPCT国際出願を以下に“なし”の欄に印をつけることにより明記する：

Prior foreign applications

先の外国出願

JP 10-45396

(番号)

Japan

(国名)

26/February/1998

Priority claimed

優先権の主張

Yes

□

あり

なし

(番号)

JP 10-45397

(番号)

Japan

(国名)

26/February/1998

Yes

□

あり

なし

(番号)

その他の外国特許出願番号は別紙の追補優先権欄に記載する。

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated
below next to my name.

I believe I am the original, first and sole inventor (if only one name is
listed below) or an original, first and joint inventor (if plural names
are listed below) of the subject matter which is claimed and for
which a patent is sought on the invention entitled

MULTILAYER PRINTED WIRING BOARD WITH FILLED
VIAHOLE STRUCTURE

the specification of which is attached hereto unless the following
box is checked:

was filed on _____ as

United States Application Number _____

and was amended on _____ (if applicable) or,

PCT International Application Number PCT/JP99/00504

and was amended on March 14, 2000 (if applicable).

I hereby state that I have reviewed and understand the contents
of the above identified specification, including the claims, as
amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to
patentability as defined in Title 37, Code of Federal Regulations,
§1.56.

I hereby claim foreign priority under Title 35, United States Code
§119(a-d) or §365(b) of any foreign application(s) for patent or
inventor's certificate, or §365(a) of any PCT International application
which designated at least one country other than the United States,
listed below. I have also identified below, by checking the "No"
box, any foreign application for patent or inventor's certificate, or of
any PCT international application having a filing date before that of
the application on which priority is claimed:

Priority claimed

優先権の主張

Yes

□

あり

なし

Yes

□

あり

なし

Additional foreign application numbers are listed on a
supplemental priority sheet attached hereto.

Declaration — Supplemental Priority Data Sheet

特許出願宣言書 — 補足優先データ表

Additional foreign applications:

その他の外国特許出願

Prior Foreign Application Number(s) 先の外国特許出願番号	Country 国名	Foreign Filing Date (DD/MM/YYYY) 外国出願年月日	Priority Claimed 優先権の主張		Certified Copy Attached? 優先権証明書は添付されたか否か?	
			YES はい	NO いいえ	YES はい	NO いいえ
JP 10-45398	Japan	26/02/1998	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
JP 10-45399	Japan	26/02/1998	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Additional provisional applications:

その他の合衆国仮特許出願

Application Number 出願番号	Filing Date (DD/MM/YYYY) 出願の年月日

Additional U.S. applications:

その他の合衆国特許出願

U.S. Parent Application Number 合衆国親出願番号	PCT Parent Number PCT親出願番号	Parent Filing Date (DD/MM/YYYY) 親出願年月日	Parent Patent Number (if applicable) 親特許番号 (該当する場合)

Japanese Language Utility or Design Patent Application Declaration

私は、合衆国法典第35部第119条(e)項に基づく、下記の合衆国仮特許出願の利益を主張する。

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

(Application No.)
(出願番号)

(Day/Month/Year Filed)
出願の年月日

(Application No.)
(出願番号)

(Day/Month/Year Filed)
出願の年月日

(Application No.)
(出願番号)

(Day/Month/Year Filed)
出願の年月日

その他の合衆国仮特許出願番号は別紙の追補優先権欄にて記載する。

私は、合衆国法典第35部第120条に基づく下記の合衆国特許出願、又は第365条(c)項に基づく合衆国を指名したPCT国際出願の利益を主張し、本欄の請求の範囲各項に記載の主題が合衆国法典第35部第112条第1項規定の範囲で、先の合衆国特許出願又はPCT国際出願に開示されていない限界において、先の出願の出願日と本願の国内出願日又はPCT国際出願日の間に有効となった連邦規則法典第37部第1章第56条に記載の特許要件に所要の情報を開示すべき義務を有することを認める。

<input type="checkbox"/>	(Application No.) (出願番号)	(Day/Month/Year Filed) (出願の年月日)	(現況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)
<input type="checkbox"/>	(Application No.) (出願番号)	(Day/Month/Year Filed) (出願の年月日)	(現況) (特許済み、係属中、放棄済み)	(Status) (patented, pending, abandoned)

その他の合衆国又は国際特許出願番号は別紙の追補優先権欄にて記載する。

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従つて行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第1部第1001条により、罰金もしくは禁錮に処せられるか、またはこれらの罰が併科され、またかかる故意による虚偽による陳述が本願ないし本願に対し付与される特許の有効性を損なうことがあることを認識して、以上の陳述を行ったことを宣言する。

私は、下記署名者は、ここに記載の米国弁護士または代理人に本出願に關し特許商標局にて取られるいかなる行為に關して、同米国弁護士又は代理人が、私に直接連絡なしに私の外国弁護士或いは法人代表者からの指示を受け取り、それに従うようここに委任する。この指示を出す者が変更の場合には、ここに記載の米国弁護士又は代理人にその旨通知される。

Additional provisional application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The undersigned hereby authorizes the U.S. attorney or agent named herein to accept and follow instructions from either his foreign patent agent or corporate representative, if any, as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U.S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorney or agent named herein will be so notified by the undersigned.

Japanese Language Utility or Design Patent Application Declaration

委任状： 私は、下記発明者として、下記に明記された顧客番号を伴う以下の弁護士又は、代理人をここに選任し、本願の手続きを行ふること並びにこれに関する一切の行為を特許商標局に対して行ふことを委任する。そして全ての通信はこの顧客番号宛に発送される。

顧客番号 7055

現在選任された弁護士は下記の通りである。

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国籍			Citizenship <u>Japan</u>
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同第2共同発明者の署名	日付		Second Inventor's signature <u>Ken-ichi Shimada</u> Date <u>00/July/13</u>
住所			Residence <u>Ibi-gun, Gifu, Japan</u>
国籍			Citizenship <u>Japan</u>
郵便の宛先			Post Office Address <u>c/o IBIDEN Co., Ltd.,</u> <u>1-1, Kitakata, Ibigawa-cho, Ibi-gun, Gifu</u> <u>501-0601 Japan</u>

(第六またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。)

(Supply similar information and signature for third and subsequent joint inventors.)

Japanese Language Utility or Design Patent Application Declaration

第三の共同発明者の氏名 共同発明者の署名 住所 国籍 郵便の宛先	3-cc 日付 Residence Citizenship Post Office Address	Full name of third inventor, if any Motoo ASAI Third Inventor's signature Motoo Asai Residence Ibi-gun, Gifu, Japan 〒191 Citizenship Japan c/o IBIDEN Co., Ltd., 1-1, Kitakata, Ibigawa-cho, Ibi-gun, Gifu 501-0601 Japan	Date
第四の共同発明者の氏名 共同発明者の署名 住所 国籍 郵便の宛先	日付	Full name of fourth inventor, if any Fourth Inventor's signature	Date
第五の共同発明者の氏名 共同発明者の署名 住所 国籍 郵便の宛先	日付	Full name of fifth inventor, if any Fifth Inventor's signature	Date
第六の共同発明者の氏名 共同発明者の署名 住所 国籍 郵便の宛先	日付	Full name of sixth inventor, if any Sixth Inventor's signature	Date

(それ以降の共同発明者にたいしても同様な情報
および署名を提供すること。)

(Supply similar information and signature for subsequent joint
inventors.)